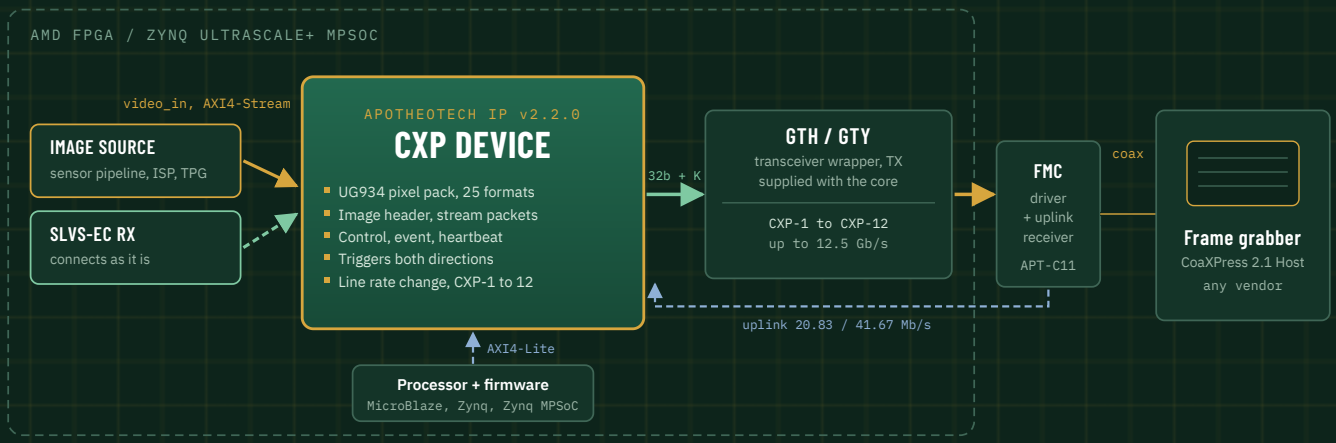
APOTHEOTECH

IP CORE DATASHEET
APT-DS-CXP-DEV-0001
Rev 1.0 · IP v2.2.0
November 2026

COAXPRESS 2.1 CAMERA CORE FOR AMD FPGAS

CoaXPress 2.1 Device IP Core

Turns UG934 AXI4-Stream video into a CoaXPress 2.1 downlink at CXP-1 to CXP-12 on GTH or GTY transceivers, in up to 25 pixel formats, with the image header, control acknowledges, events, heartbeat, triggers and line rate change handled in hardware.



12.5 Gb/s
per connection, CXP-12

25
pixel formats, built by switch

TX only
GTH option, frees the receivers

Any Host
CoaXPress 2.1 frame grabbers

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SECTION 01

Overview

A CoaXPress 2.1 Device link layer for AMD FPGAs, from UG934 AXI4-Stream video to the coax.

1.1 Introduction

The ApotheoTech CoaXPress 2.1 Device IP Core implements the Device link layer of the JIIA CXP-001-2021 CoaXPress standard, version 2.1: the side of the link that sits in a camera and sends video to a frame grabber. It drives the GTH or GTY transmitter of an AMD UltraScale+ device through a transceiver wrapper supplied with the core, and receives the low-speed uplink from the frame grabber through the CoaXPress front end on the board.

Your image pipeline hands the core a UG934 AXI4-Stream. The core packs the pixels in the CoaXPress format of the selected pixel type, adds the rectangular image header and the line markers, cuts the stream into packets and sends them, with acknowledges, events, heartbeats and triggers interleaved by priority. Control commands from the frame grabber are handed to firmware, which owns the camera's register space and GenICam description and answers through the acknowledge builder. A line rate change is a single register write.

The **GTH transmitter only** option uses only the transmit side of a transceiver, so the receivers of the same quad stay free for an SLVS-EC or other sensor interface. The default video bus is the 64-bit, 4-pixel beat of the ApotheoTech SLVS-EC Receiver, so a sensor stream connects to the Device core as it is.

1.2 Features

LINK LAYER

- CoaXPress 2.1 Device (JIIA CXP-001-2021)
- CXP-1 to CXP-12: 1.25 to 12.5 Gb/s on one connection
- IDLE word at least every 100 words, as CoaXPress 2.1 requires
- Uplink receiver with byte and word lock, following 20.83 and 41.67 Mb/s by itself
- Line rate change in hardware: DRP rewrite, PLL reset, retries and an error code
- GTH, GTY, or GTH transmitter only; wrapper supplied with the core

PROTOCOL

- Rectangular image header and line markers built from registers, taken at stream on
- Stream packets up to StreamPacketSizeMax, with tag and CRC
- Control commands received into a FIFO for firmware; acknowledges built from registers
- Event packets built from registers; the Host's acknowledge reported
- Heartbeat with a 64-bit nanosecond time stamp and the Host ID
- Triggers both directions, uplink triggers acknowledged by the core or by firmware; connection test

VIDEO INPUT

- UG934 AXI4-Stream video slave: `tuser` start of frame, `tlast` end of line, on its own clock
- 2 or 4 pixels per beat, 8 to 16 bits per component, 1 to 3 components per pixel
- Mono, Bayer and Raw; RGB; YCbCr 4:4:4, 4:2:2 and 4:2:0; 8, 10, 12, 14 and 16-bit on the link

INTEGRATION

- AXI4-Lite control in a 4 KB window with ID, version and build discovery
- Interrupt controller with status, enable, pending and software test registers
- Word, register, uplink and video clocks independent; all crossings inside the core

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- Each layout and bit depth built only when switched on in the IP GUI
- Format selected at run time by one register write
- Line and frame size checked against the image header
- Packaged for Vivado IP Integrator with a customization GUI
- Firmware driver for MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC
- Example designs on ZCU106 with the APT-C11-FMC CoaXPress card

1.3 Key specifications

Table 1-1. Key specifications of the CoaXPress 2.1 Device IP Core v2.2.0.

Standard	JIIA CXP-001-2021, CoaXPress 2.1, Device link layer
Connections	1 (one coax). Builds for 2 and 4 connections on request
Speeds	CXP-1, CXP-2, CXP-3, CXP-5, CXP-6, CXP-10, CXP-12: 1.25 to 12.5 Gb/s, changed at run time
Uplink	20.83 and 41.67 Mb/s, received through the CoaXPress front end on the board
Transceiver	AMD UltraScale+ GTH (GTHE4), GTH transmitter only, or GTY (GTYE4), through the supplied transceiver wrapper
Video input	AXI4-Stream slave, AMD UG934 video convention, on its own clock
Bus	2 or 4 pixels per beat (`VID_PPC`), 8 to 16 bits per component (`VID_BPC`), 1 to 3 components (`VID_CPP`); `tdata` 16 to 192 bits, default 64
Pixel formats	Mono / Bayer / Raw, RGB, YCbCr 4:4:4, 4:2:2, 4:2:0 (sent as 4:2:2); 8, 10, 12, 14, 16-bit on the link; up to 25 per build
Pixel rate	Up to 1,220 Mpx/s on one CXP-12 connection (Mono 8-bit, 4 pixels per beat)
Protocol	Stream with image header, control acknowledges (tagged and untagged), events, heartbeat, triggers both directions, connection test
Control interface	AXI4-Lite slave, 32-bit data, 12-bit address (4 KB), 57 registers
Interrupt	`cxp_dev_int`, 14 sources, level with a re-arm gap after each status write
Clocks	Word clock from the transceiver = line rate / 40 (312.5 MHz at CXP-12); AXI4-Lite clock 50 to 250 MHz; video and uplink clocks independent
Target devices	AMD Zynq UltraScale+ MPSoC, Kria K26 SOM and Kintex UltraScale+; other UltraScale+ devices with GTH or GTY transceivers
Software	Firmware driver for MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC, supplied on purchase
Design flow	AMD Vivado Design Suite, IP Integrator or RTL instantiation

1.4 Throughput

The core keeps the link full at every speed. The pixel path runs on the word clock and fills one 32-bit link word per clock, so at 4 pixels per beat it carries every format at the full rate of the connection. At 2 pixels per beat only Mono and Bayer formats below 16 bits leave link capacity unused.

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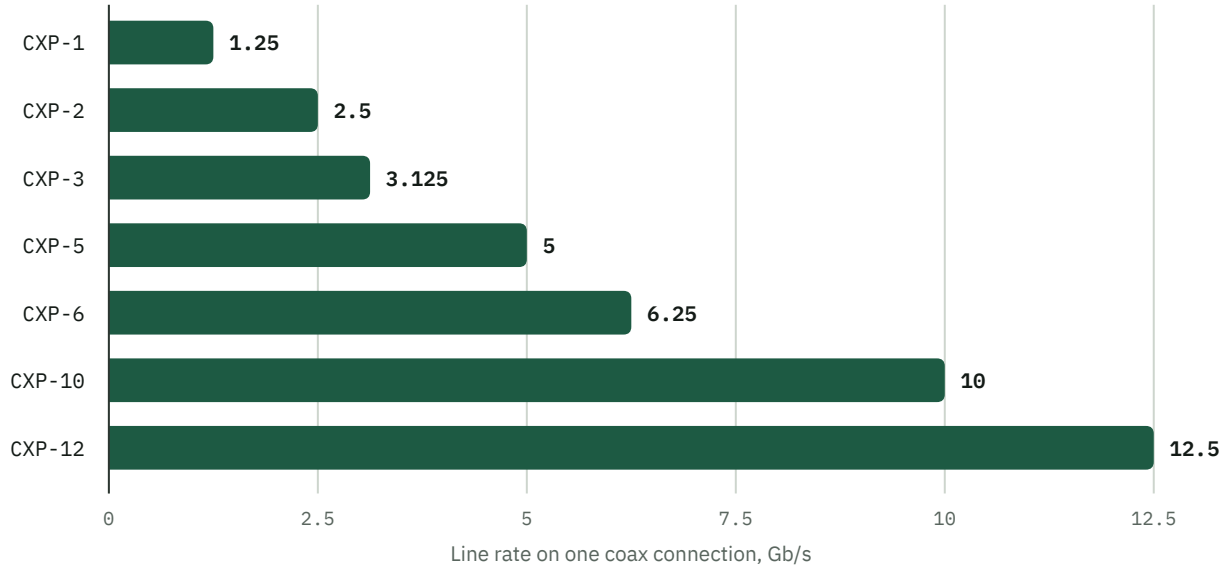


Figure 1-1. Line rate per CoaXPress speed on one connection. Hover a bar for the payload rate and the uplink rate.

Table 1-2. CoaXPress speeds on one connection. The word clock is the line rate / 40 (one 32-bit word per clock); payload is the line rate after 8b/10b decoding, before packet overhead.

SPEED	LINE RATE GB/S	PAYLOAD GB/S	PAYLOAD MB/S	WORD CLOCK MHZ	UPLINK MB/S
CXP-1	1.25	1	125.0	31.25	20.83
CXP-2	2.5	2	250.0	62.5	20.83
CXP-3	3.125	2.5	312.5	78.125	20.83
CXP-5	5	4	500.0	125	20.83
CXP-6	6.25	5	625.0	156.25	20.83
CXP-10	10	8	1,000.0	250	41.67
CXP-12	12.5	10	1,250.0	312.5	41.67

1.5 Applications

Machine vision cameras
CoaXPress output for area and line scan sensors

Sensor bridges
SLVS-EC, MIPI or LVDS sensors to CoaXPress

High-speed cameras
CXP-12 from a Zynq MPSoC or Kintex pipeline

Smart cameras
On-camera ISP and processing, CoaXPress out

Scientific cameras
Deterministic delivery with triggers both ways

Test equipment
Pattern sources for frame grabber test and production

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Camera emulators
Replay recorded video as a CoaXPress camera

Video bridges
SDI, HDMI or Ethernet video to CoaXPress

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SECTION 02

Functional Description

How the Device core turns AXI4-Stream video into a CoaXPress downlink and serves the frame grabber: the transmit path, the video bus and pixel formats, control and acknowledges, events, heartbeat, triggers, line rate change, interrupts and clocks.

2.1 Architecture

The core is the Device link layer. Video enters on an AXI4-Stream on your clock and crosses to the word clock of the transceiver, where it is packed, framed and sent as 32-bit words with K flags to the supplied transceiver wrapper. The uplink from the frame grabber enters on its own receiver. Firmware sees everything else through the register file.

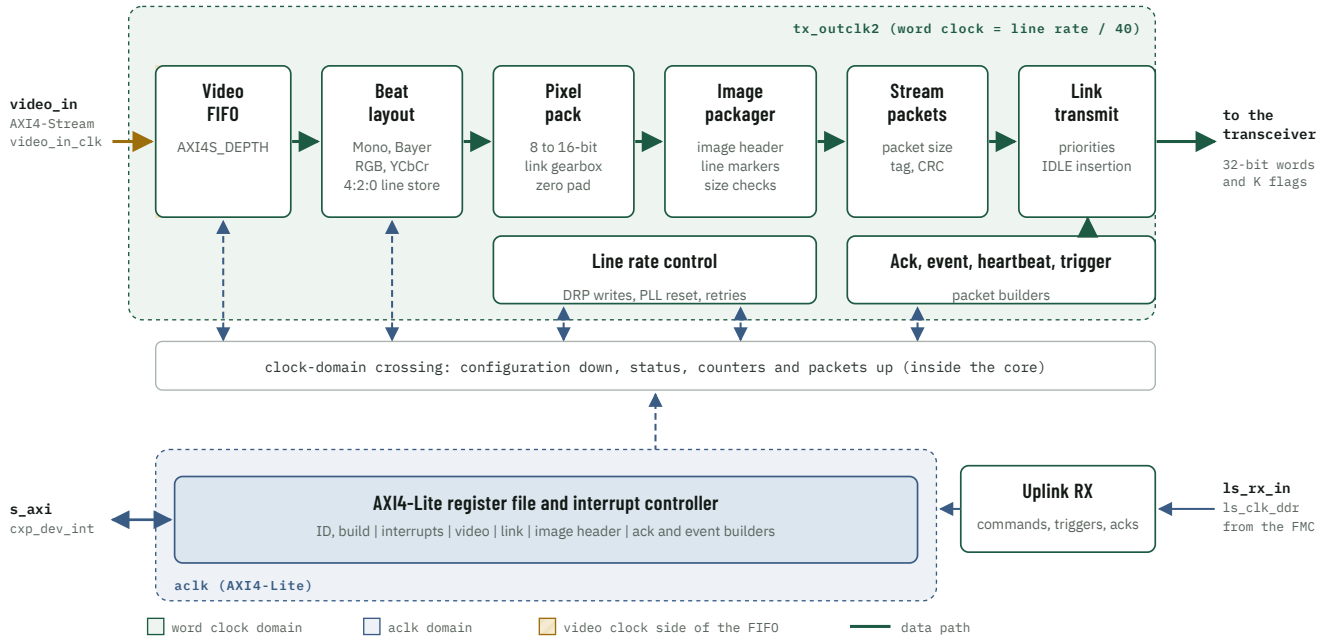


Figure 2-1. Functional block diagram. The transmit path runs on the transceiver word clock; the register file and the interrupt controller run on the AXI4-Lite clock; the video FIFO is written on the video clock; the uplink receiver runs on the clock recovered from the uplink. All crossings are inside the core.

01 Video FIFO

Takes the UG934 beats on `video_in_clk` and crosses them to the word clock.

02 Beat layout

Takes the components of each pixel off the beat in the order of the selected layout; for YCbCr 4:2:0 a line store repeats the chroma of each even line on the odd line after it.

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03 Pixel pack
Packs the components at the bit depth of the link, 8 to 16 bits, in the CoaXPress order, and pads the last word of each line with zeros.

04 Image packager
Adds the rectangular image header and the line markers from the image registers, and checks every line and frame against them.

05 Stream packets
Cuts the stream into packets of at most StreamPacketSizeMax bytes with stream ID, packet tag, size and CRC.

06 Link transmit
Interleaves triggers, acknowledges, events, heartbeats and stream packets by priority and inserts an IDLE word at least every 100 words.

2.2 Transceiver and link

The core runs on an AMD UltraScale+ transceiver, selected with **Transceiver** in the IP GUI:

Table 2-1. Transceiver options.

OPTION	USES	USE IT WHEN
GTH, transmitter only `default`	The transmit side of a GTH channel	The receivers of the quad serve something else, such as the lanes of an SLVS-EC sensor
GTH	A GTH channel	Zynq UltraScale+ MPSoC, Kria and Kintex devices with GTH
GTY	A GTY channel	Kintex and Virtex UltraScale+ devices with GTY

The transceiver wrapper is delivered with the core, set up for CoaXPress: line rates, 8b/10b and the DRP rate tables the core uses for a line rate change. The coax needs a CoaXPress cable driver and an uplink receiver between the FPGA and the connector, as on the APT-C11-FMC; the core takes the uplink bit stream on `ls_rx_in` with its clock on `ls_clk_ddr`.

- **Downlink.** At least one IDLE word every 100 words (**Words between IDLE words**, 99 by default as CoaXPress 2.1 allows; 64 and 32 are available). Packets are sent by priority: triggers first, then acknowledges, events, heartbeats and stream data.
- **Uplink.** The receiver finds byte lock, then word lock on IDLE words, and follows 20.83 and 41.67 Mb/s by itself. LS_RX_ALIGNED reports a Host on the line; loss of byte or word lock raises its own interrupt. The lock thresholds are set on the Advanced page of the IP GUI.
- **Connections.** The IP package builds one connection. Builds with 2 and 4 connections are available on request.

2.3 Video bus

The video input is an AXI4-Stream slave in the AMD UG934 video convention, the same beat the ApotheoTech Host core puts out, so what enters the Device leaves the Host bit for bit when both are built with the same `VID_PPC` and `VID_BPC`:

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01 Pixel order
Pixel 0, the first in time, sits in the least significant bits. Pixels are packed tight.

02 Component order
A pixel is its components packed tight, in the UG934 order of its layout.

03 Component width
Every component has `VID_BPC` bits on the bus. When the link depth is narrower, the top bits are sent and the LSBs ignored; when it is wider, the LSBs on the link are zero.

04 Padding
`tdata` is padded to a whole number of bytes; bits a format does not use are ignored.

05 Framing
`tuser[0]` marks the first beat of a frame, `tlast` the last beat of every line.

Table 2-2. `tdata` width in bits by components per pixel (`VID_CPP`), pixels per beat (`VID_PPC`) and bits per component (`VID_BPC`). The IP GUI derives it from the format switches. Shaded: the default.

VID_CPP	VID_PPC	BPC 8	BPC 10	BPC 12	BPC 14	BPC 16
1 Mono, Bayer, Raw	2	16	24	24	32	32
	4	32	40	48	56	**64**
2 adds YCbCr 4:2:2 and 4:2:0	2	32	40	48	56	64
	4	64	80	96	112	128
3 adds RGB and YCbCr 4:4:4	2	48	64	72	88	96
	4	96	120	144	168	192

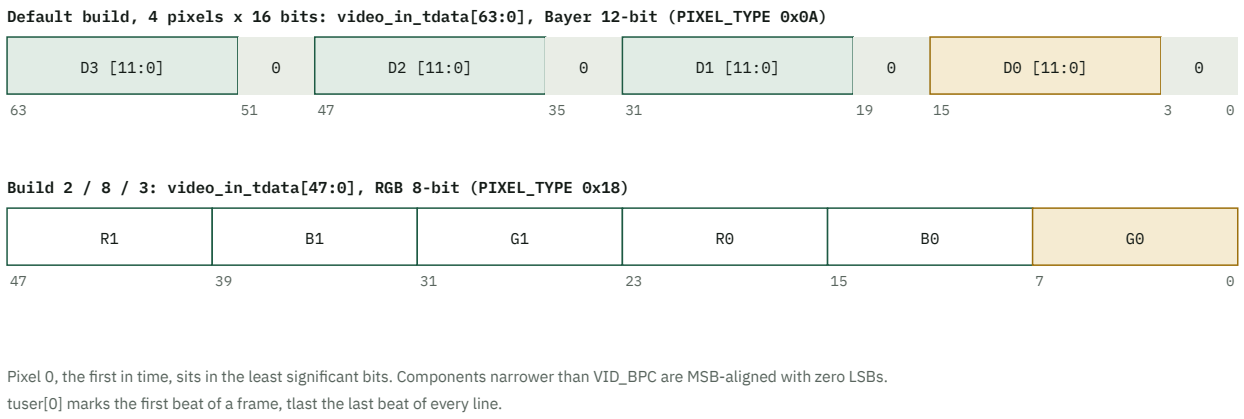


Figure 2-2. Two video beats: the default 64-bit build carrying Bayer 12-bit, and a 2 / 8 / 3 build carrying RGB 8-bit.

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The default bus, 4 pixels of 16 bits on 64 bits, is the beat of the ApotheoTech SLVS-EC Receiver at 2 lanes: 16-bit containers, MSB-justified, first pixel in container 0. The sensor stream connects to `video_in` as it is, at every bit depth. AMD video IP connects directly when it uses the same samples per clock, data width and number of components.

2.4 Pixel formats

Firmware selects the format in `PIXEL_TYPE` and writes the matching CoaXPress pixel format code into the image header registers. The code is {layout, bit depth on the link}:

Table 2-3. `PIXEL_TYPE` codes: bits [7:4] select the layout, bits [3:0] the bit depth on the link (8 = 8-bit to C = 16-bit). 0x00 is accepted as RGB 8-bit, the code of earlier releases.

LAYOUT	8-BIT	10-BIT	12-BIT	14-BIT	16-BIT	COMPONENTS, LSB FIRST	BUILT BY
Mono / Bayer / Raw	0x08	0x09	0x0A	0x0B	0x0C	the sample	VID_EN_MONO
RGB	0x18	0x19	0x1A	0x1B	0x1C	G, B, R	VID_EN_RGB
YCbCr 4:4:4	0x28	0x29	0x2A	0x2B	0x2C	Y, Cb, Cr	VID_EN_YCBCR444
YCbCr 4:2:2	0x38	0x39	0x3A	0x3B	0x3C	Y, C (Cb even pixels, Cr odd)	VID_EN_YCBCR422
YCbCr 4:2:0	0x48	0x49	0x4A	0x4B	0x4C	Y, C (C on even lines only)	VID_EN_YCBCR420

- **Built by switch.** Each layout has a switch in the IP GUI and **Bit depths on the link** picks the depths. Mono / Bayer at every depth is the default. With everything on, one build carries 25 formats. `VIDEO_CAP` reports what was built, and `PIXEL_TYPE.NOT_BUILT` flags a code the bitstream has no path for.
- **Run-time selection.** A write to `PIXEL_TYPE` restarts the pixel packers with the new format. Write it with the acquisition stopped.
- **YCbCr 4:2:0.** CoaXPress has no packed 4:2:0 format. The core takes UG934 4:2:0 on `video_in`, keeps the chroma of each even line in a line store and sends it again with the odd line, so the link carries a normal YCbCr 4:2:2 picture that any Host shows. The store is sized by **Widest YCbCr 4:2:0 line**, 1,024 to 16,384 pixels: two BRAM36 at the default 4,096.

2.4.1 Lines and frames

- A line is a multiple of 4 pixels; for YCbCr 4:2:2 and 4:2:0 a multiple of `VID_PPC` is enough.
- Every line starts in a new link word, and the last word of a line is zero-padded as CoaXPress 2.1 requires.
- Everything before the first `tuser` is discarded, so the first frame sent is a whole frame. A `tuser` inside a line starts a new frame and is flagged.
- Line and frame size are checked against `CXP_IMG_XSIZE` and `CXP_IMG_YSIZE`; a mismatch sets an error flag in `CXP_ERRORS_HS`.

2.4.2 Throughput

Table 2-4. Pixel path throughput: share of the link words of one connection the path takes per word clock, and the pixel rate one CXP-12 connection carries.

FORMAT	2 PIXELS PER BEAT	4 PIXELS PER BEAT	MPX/S AT CXP-12
Mono / Bayer 8-bit	50 %	100 %	1220

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FORMAT	2 PIXELS PER BEAT	4 PIXELS PER BEAT	MPX/S AT CXP-12
Mono / Bayer 10-bit	62 %	100 %	976
Mono / Bayer 12-bit	75 %	100 %	813
Mono / Bayer 14-bit	87 %	100 %	697
Mono / Bayer 16-bit	100 %	100 %	610
YCbCr 4:2:2 8 / 10 / 12-bit	100 %	100 %	610 / 488 / 407
RGB or YCbCr 4:4:4 8 / 10 / 12-bit	100 %	100 %	407 / 325 / 271

The video clock must carry the pixel rate: `video_in_clk` ≥ pixels per second / `VID_PPC`. When the link is slower than the source, `video_in_tready` pushes back; size the source's own buffering for the frame rate the link carries.

2.5 Image header and stream

The rectangular image header is built from registers: `CXP_IMG_XSIZE`, `CXP_IMG_XOFFS`, `CXP_IMG_YSIZE`, `CXP_IMG_YOFFS`, `CXP_IMG_BPP`, `CXP_RECT_PIXELF`, `CXP_RECT_TAPG` and `CXP_RECT_FLAGS`. They reset to the core's defaults (3840 x 2160, 8 bits per pixel, BayerRG8) and are taken when firmware starts the stream:

01 Configure
Write the image registers, `PIXEL_TYPE` and `CXP_STREAM_PCKT_MAX` with the packet size agreed with the Host.

02 Stream on
Write `STREAM_STATUS` bit 0. The stream path takes the image registers and confirms; STREAM_ON fires and `CXP_STATUS.HS_STREAM_ACTIVE` rises.

03 Stream off
Write `STREAM_STATUS` bit 1. The frame in flight is finished, then STREAM_OFF fires.

If the stream path does not confirm an on or off request within `ACK_TIMEOUT`, `CXP_TIMEOUTS` records it and ACK_ERR fires. The same applies to test packets on and off.

2.6 Control channel

A CoaXPress camera answers the frame grabber's register reads and writes: the bootstrap registers, the GenICam description and the camera's own features. The Device core receives each command and hands it to firmware, which owns the register space and answers:

01 Receive
LS_CNTRL_VLD fires when a command is in. Read the command and size, the address, the tag (CXP 2.x), and for a write the data words from `CXP_CTRL_RX_FIFO`. Commands with a CRC error are counted in `LS_RX_CNTRL_CRC_ERRS` and flagged in `CXP_CTRL_RX_ERR`.

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02 **Answer**
Write the acknowledge code, the size, the tag received with the command and, for a read, the data words to `CXP_CTRL_ACK_FIFO`.

03 **Send**
Write `CXP_CTRL_ACK_SEND`. Errors in an acknowledge built this way are flagged in `CXP_ERRORS_HS[6:0]`.

`CXP_LS_MODE` bit 0 selects CoaXPress 2.x operation: tagged commands and the heartbeat. The supplied firmware driver reads the commands and sends the acknowledges; the camera application implements the bootstrap registers, its own features and its GenICam description, as the example design shows.

2.7 Events, triggers and heartbeat

Table 2-5. Asynchronous traffic.

FUNCTION	DIRECTION	BEHAVIOUR
Events	Camera to Host	Firmware writes the tag, size and data words and sends the event with `CXP_EVENT_SEND`. The Host's acknowledge raises LS_EVENT_ACK_VLD and its tag is in `CXP_EVENT_ACK`.
Triggers from the Host	Host to camera	An uplink trigger raises LS_TRIG; its number and delay are in `CXP_LS_RX_TRIG`. The core acknowledges it by default (**Trigger acknowledge** = By the core), or firmware does with `CXP_TRIG_SEND.SEND_ACK`.
Triggers to the Host	Camera to Host	`CXP_TRIG_SEND.SEND_TRIG` sends a high-speed trigger with the indication in bits [7:0]; the Host's acknowledge raises LS_TRIG_ACK.
Heartbeat	Camera to Host	Sent every 10, 20, 50 or 100 ms (**Heartbeat period**) in CXP 2.x mode, with the Host ID from `CXP_TX_MSTR_ID` and the 64-bit Device time in nanoseconds. The time advances by `CXP_HRTBT_CNTR_INCR` each aclk cycle and can be set by firmware.
Connection test	Both	`CXP_TEST_PCKT_MODE` sends test packets on the downlink and counts them; test packets on the uplink are checked and counted good or bad.

2.8 Line rate change

The frame grabber discovers the camera at a low speed and moves it to the operating speed with ConnectionConfig. When firmware has acknowledged that write, it writes the new speed code and `CXP_RATE_TRANS.APPLY`. The core then

01 **Rewrites the transmitter**
DRP writes to the channel and common PLL for the new rate, from tables built into the core for each transceiver option.

02 **Resets it**
A PLL and datapath reset on `reset_TX_PLL`, held at least the minimum time.

03 **Waits for it**
The transmitter must take the reset and report reset done within the timeouts set in the IP GUI; the core retries the reset up to the configured number of times.

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04 Reports
TX_READY when the transmitter is back, or RATE_ERR with an error code in `CXP_STATUS[15:14]`.

A request is taken in any state, also with the transmitter down, and a request during a change runs next (newest wins). The core refuses rate code 7 with SLVERR.

Table 2-6. Line rate change error codes, `CXP_STATUS[15:14]`. After an error the core is idle again and takes the next request.

CODE	MEANING	WHAT TO CHECK
1	**DRP no answer**	The transceiver did not answer the DRP writes in time. The transceiver is not reset; check the DRP clock and connection.
2	**Reset not acknowledged**	The transceiver wrapper never took the PLL and datapath reset: `reset_TX_PLL` is not connected to it.
3	**Reset done never back**	`transmitter reset done` did not return after the retries: the PLL is not locking (reference clock, or the board).

2.9 Interrupts

Fourteen sources feed one interrupt output, `cxp_dev_int`. `ISR` holds a sticky bit per source whether or not it is enabled, `IER` enables sources, `IPR` = ISR and IER shows what drives the output, `GLBL_IER` gates the output, and `IRQ_TEST` sets ISR bits from software. The output is a level; after every write to `ISR` it drops for four clocks and returns if anything is still pending, so an edge-triggered input sees every event too. The bit list is in ISR.

2.10 Buffering

Table 2-7. Buffers, set in the IP GUI.

BUFFER	GUI FIELD	SIZES	HOLDS
Video input FIFO	Video input FIFO (beats)	`512 to 4096`	Beats crossing from the video clock
Packager FIFO	Packager FIFO (words)	`512 to 4096`	Packed words waiting for the image packager
Stream packet FIFO	Stream packet FIFO (words)	`8192, 16384, 32768`	Stream packets waiting for the link
Acknowledge FIFOs	Control acknowledge FIFOs (words)	`4096, 8192`	Acknowledge data from firmware
Event FIFOs	Event FIFOs (words)	`512, 1024, 2048`	Event data from firmware
Command FIFO	Control command FIFO (words)	`4096, 8192`	Write data of received control commands

The defaults suit the example designs. Deeper FIFOs cost block RAM only.

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2.11 Clocks and reset

Table 2-8. Clock domains.

CLOCK	SOURCE	RUNS
`tx_outclk2`	Word clock from the transceiver wrapper: line rate / 40, 312.5 MHz at CXP-12; changes with the speed	Pixel path, packagers, link transmit
`aclk`	Free-running clock, 50 to 250 MHz, set in the GUI; also the time base of the heartbeat and the acknowledge timeouts	Register file, interrupt controller, line rate change, heartbeat time
`video_in_clk`	The clock of your video source, any frequency that carries the pixel rate	The write side of the video FIFO and `video_in`
`ls_clk_ddr`	Clock of the uplink from the CoaXPress front end	Uplink receiver
`drp_clk`	DRP clock of the transceiver wrapper	DRP accesses for the line rate change

- Clock `aclk` from a free-running clock and set **AXI4-Lite clock** in the GUI to its frequency: the heartbeat period, the time stamp and the timeouts depend on it.
- Every crossing uses AMD XPM macros and constrains itself. Enable the XPM libraries in the project; do not add clock groups or false paths between these clocks.
- `reset_TX_PLL` must reach the PLL and datapath reset of the transceiver wrapper, as in the example designs. Without it a line rate change ends with error code 2 or 3.
- `RST_CXP` pulses resets for the whole core or one path (stream, acknowledges, events, heartbeat, command receiver, uplink), so firmware can recover a part without a reconfiguration.

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SECTION 03

Interfaces and Timing

IP parameters by GUI page, every interface of the core, the video input timing and the integration checklist.

3.1 IP customization parameters

Every setting in the IP GUI is a drop-down list; fields the GUI works out are shown read-only. Firmware reads the build back from `HWCFG` and `VIDEO_CAP`. Defaults are in bold.

3.1.1 Link

Table 3-1. Link page.

GUI FIELD	PARAMETER	VALUES	DESCRIPTION
Transceiver	TRANSCEIVER_TYPE	**GTH, transmitter only**, GTH, GTY	Transceiver option and its DRP rate tables.
Connections	NUM_LANES	**1**	Coax connections. 2 and 4 on request.
AXI4-Lite clock (aclk)	ACLK_FREQ_MHZ	50, **100**, 125, 200, 250 MHz	Frequency of `aclk`: time base of the heartbeat, the acknowledge timeouts and the line rate change.
Trigger acknowledge	PASSTHRU_TRIG	**By the core**, By software	Who acknowledges a trigger from the Host.
Heartbeat period (ms)	HRTBT_SEND_PERIOD	**10**, 20, 50, 100	Time between heartbeats in CXP 2.x mode.
Acknowledge timeout after reset (ms)	ACK_WAIT_DEF_MS	10, **33**, 50, 100, 200	Reset value of `ACK_TIMEOUT`.

3.1.2 Video

Table 3-2. Video page.

GUI FIELD	PARAMETER	VALUES	DESCRIPTION
Mono / Bayer	VID_EN_MONO	**Built**, Not built	Mono, Bayer and Raw layouts, 1 component.
RGB	VID_EN_RGB	Built, **Not built**	RGB, 3 components.
YCbCr 4:4:4	VID_EN_YCBCR444	Built, **Not built**	3 components.
YCbCr 4:2:2	VID_EN_YCBCR422	Built, **Not built**	2 components.
YCbCr 4:2:0	VID_EN_YCBCR420	Built, **Not built**	4:2:0 on the bus, 4:2:2 on the link.
Widest YCbCr 4:2:0 line (pixels)	VID_420_MAX_WIDTH	1024, 2048, **4096**, 8192, 16384	Size of the chroma line store.
Bit depths on the link	VID_LINK_WIDTHS	**8, 10, 12, 14 and 16-bit**, or any subset	Each depth is a gearbox of its own.
Pixels per beat	VID_PPC	2, **4**	Pixels per `video_in` beat.

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GUI FIELD	PARAMETER	VALUES	DESCRIPTION
Bits per component	VID_BPC	8, 10, 12, 14, **16**	Component width on the bus.
Components per pixel	VID_CPP	read-only, **1**	3 with RGB or YCbCr 4:4:4, 2 with YCbCr 4:2:2 or 4:2:0, else 1.
TDATA width (bit)	MAX_TDATA_WIDTH	read-only, **64**	`VID_PPC` x `VID_CPP` x `VID_BPC`, rounded up to whole bytes.
Pixel format after reset	PIXEL_TYPE_DEFAULT	25 codes, **Mono / Bayer 8-bit (0x08)**	Reset value of `PIXEL_TYPE`.

3.1.3 Buffers

Table 3-3. Buffers page.

GUI FIELD	PARAMETER	VALUES
Video input FIFO (beats)	AXI4S_DEPTH	**512**, 1024, 2048, 4096
Packager FIFO (words)	PIXEL_PCKG_DEPTH	**512**, 1024, 2048, 4096
Stream packet FIFO (words)	STREAM_PCKT_MAX_DEPTH	**8192**, 16384, 32768
Control acknowledge FIFOs (words)	HS_CNTRL_PCKT_MAX_SIZE	**4096**, 8192
Event FIFOs (words)	HS_EVENT_FIFO_DEPTH	**512**, 1024, 2048
Control command FIFO (words)	LS_CNTRL_PCKT_MAX_SIZE	**4096**, 8192

3.1.4 Advanced

Table 3-4. Advanced page.

GUI FIELD	PARAMETER	VALUES
Synchronizer flops	SYNC_STAGE	2, 3, **4**, 5, 6
Synchronizer flops, uplink receiver	LS_SYNC_STAGE	**2**, 3, 4
Words between IDLE words	IDLE_REG_MAX	**99**, 64, 32
Words without IDLE allowed	LS_IDLE_WORD_LIMIT	1000, 5000, **10000**, 20000, 50000
IDLE words for word lock	LS_WORD_IDLE_LOCK_CNTR	8, 16, **32**, 64, 128
Bad words to drop word lock	LS_WORD_LOSS_LOCK_CNTR	8, 16, **32**, 64, 128
Good characters for byte lock	LS_IDLE_BYTE_LOCK_CNTR	8, 16, **32**, 64, 128
Bad characters for the next bit slip	LS_BYTE_LOSS_LOCK_CNTR	8, 16, **32**, 64, 128
Extra reset attempts	RECONFIG_RETRIES	0, 1, **2**, 3
DRP timeout	RECONFIG_DRP_TIMEOUT_US	**1 ms**, 2, 5, 10 ms
Reset acknowledge timeout	RECONFIG_RST_ACK_TIMEOUT_US	**100 µs**, 1, 10, 100 ms

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GUI FIELD	PARAMETER	VALUES
Reset done timeout	RECONFIG_DONE_TIMEOUT_US	**20 ms**, 50, 100, 200 ms

From a block design script, for the default Bayer camera build on a GTH transmitter:

```
set_property -dict [list \
    CONFIG.TRANSCEIVER_TYPE  {GTHE4_TX_ONLY} \
    CONFIG.ACLK_FREQ_MHZ     {100} \
    CONFIG.VID_PPC           {4} \
    CONFIG.VID_BPC           {16} \
    CONFIG.HRTBT_SEND_PERIOD {10} \
] [get_bd_cells cxp_dev_0]
```

3.2 Interface overview

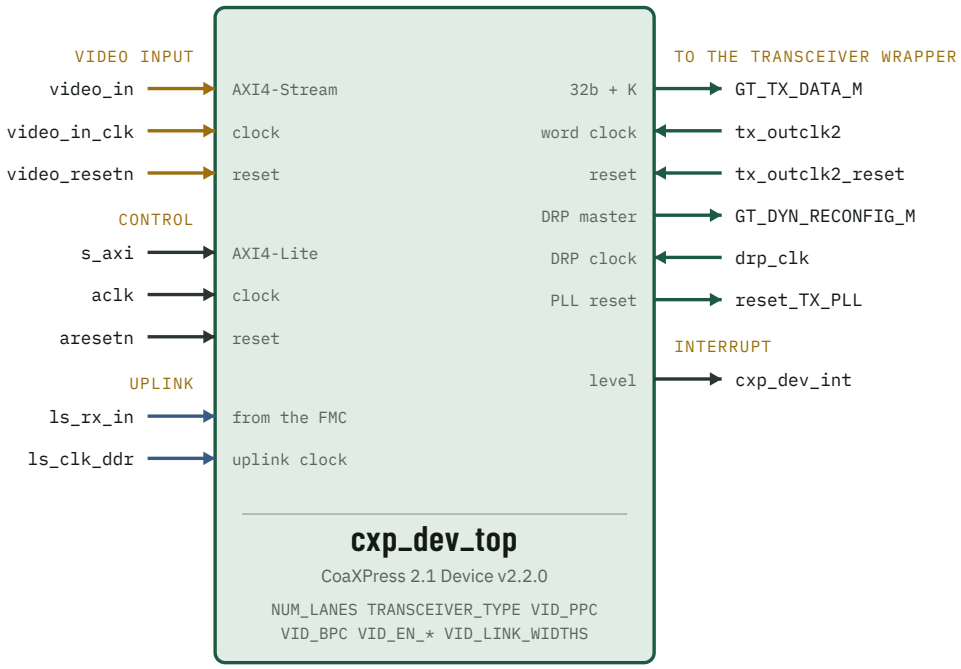


Figure 3-1. IP symbol. Gold interfaces are the video input, blue is the uplink from the FMC, green interfaces connect to the supplied transceiver wrapper, dark ones are control.

3.3 Interface descriptions

3.3.1 Video input

Table 3-5. AXI4-Stream video slave video_in.

PORT	DIR	WIDTH	DESCRIPTION

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PORT	DIR	WIDTH	DESCRIPTION
video_in_clk	in	1	Video clock, any frequency ≥ pixel rate / VID_PPC, no relation to the word clock
video_resetn	in	1	Active-low reset on video_in_clk
video_in_tdata	in	MAX_TDATA_WIDTH	UG934 beat: VID_PPC pixels, pixel 0 in the LSBs
video_in_tvalid	in	1	Beat valid
video_in_tready	out	1	Low while the video FIFO is full; the core takes a beat on every clock with both high
video_in_tuser	in	1	Start of frame: first beat of the first line
video_in_tlast	in	1	End of line: last beat of every line

3.3.2 AXI4-Lite control and interrupt

Table 3-6. Register interface and interrupt.

INTERFACE	DIR	WIDTH	DESCRIPTION
s_axi	slave	addr 12, data 32	AXI4-Lite. Write address and write data are accepted in either order. A refused access answers SLVERR (see Register interface); a read the register block does not answer within 255 clocks answers SLVERR instead of hanging the bus
aclk	in	1	Register clock, free-running; the frequency set in the GUI
aresetn	in	1	Active-low reset on aclk
cxp_dev_int	out	1	Interrupt, active high level; drops for 4 clocks after each ISR write and returns while sources are pending

3.3.3 Uplink

Table 3-7. Low-speed uplink from the CoaXPress front end.

PORT	DIR	WIDTH	DESCRIPTION
ls_rx_in	in	1	Uplink data from the front end on the FMC
ls_clk_ddr	in	1	Uplink clock recovered by the front end

3.3.4 Transceiver wrapper

Table 3-8. Connections to the supplied transceiver wrapper. Connect them as in the example designs.

INTERFACE	DIR	TYPE	DESCRIPTION
GT_TX_DATA_M	out	bus	32-bit words and K flags to the transmitter
tx_outclk2	in	clock	Word clock, line rate / 40

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INTERFACE	DIR	TYPE	DESCRIPTION
tx_outclk2_reset	in	reset	Reset of the word clock domain from the wrapper
GT_DYN_RECONFIG_M	out/in	DRP	DRP master used for the line rate change
drp_clk	in	clock	DRP clock
reset_TX_PLL	out	reset	PLL and datapath reset request. Must reach the wrapper's transmit PLL and datapath reset

3.4 Video input timing

Standard AXI4-Stream rules: the source holds `tvalid` and the payload until the handshake, and the core lowers `tready` only when its video FIFO is full. The first capture shows a whole frame of three short lines; the second shows the beat level with the core holding the source back.

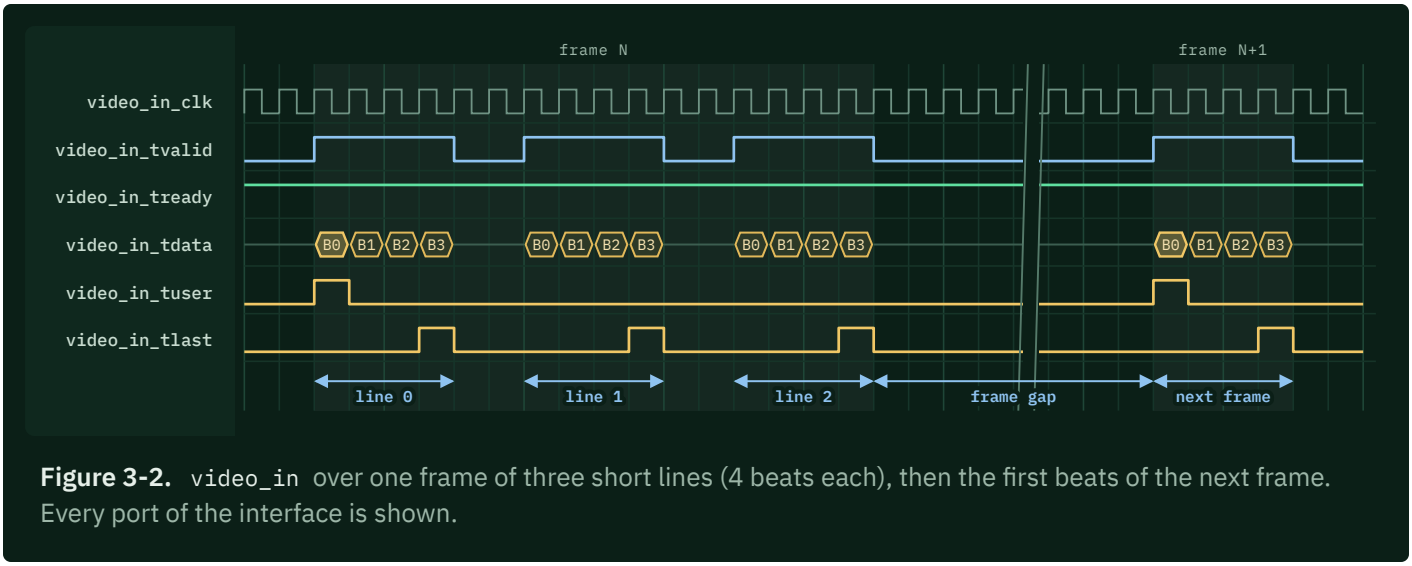


Figure 3-2. `video_in` over one frame of three short lines (4 beats each), then the first beats of the next frame. Every port of the interface is shown.

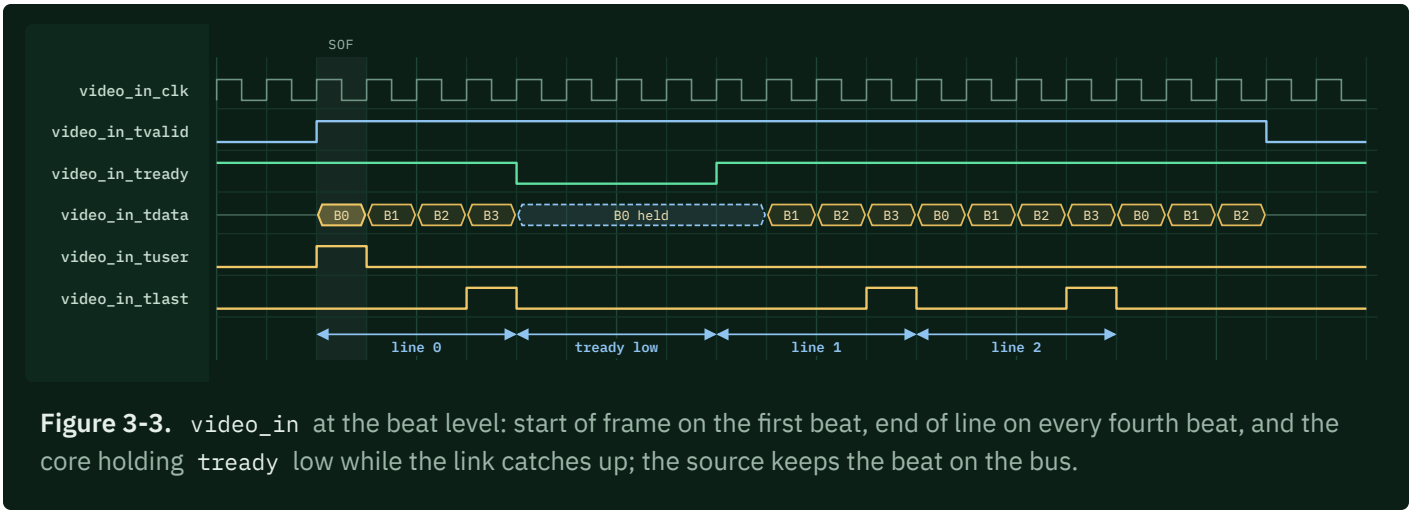


Figure 3-3. `video_in` at the beat level: start of frame on the first beat, end of line on every fourth beat, and the core holding `tready` low while the link catches up; the source keeps the beat on the bus.

3.5 Integration checklist

- XPM libraries enabled in the Vivado project.
- `reset_TX_PLL` connected to the transceiver wrapper's transmit PLL and datapath reset.

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- `cxp_dev_int` connected as a level, active high, or as an edge.
- A 4 KB address range for `s_axi` in the Vivado address editor.
- **AXI4-Lite clock** in the GUI set to the real `aclk` frequency.
- Firmware writes `PIXEL_TYPE` to the format of the video, or `PIXEL_TYPE_DEFAULT` is what the source delivers.
- Firmware writes `STREAM_LANES` on ConnectionConfig and after a ConnectionReset.
- `video_in_clk` fast enough for the pixel rate at `VID_PPC` pixels per beat.

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SECTION 04

Register Map

Fifty-seven 32-bit registers on AXI4-Lite in a 4 KB window: identification and interrupts, video, link control, the image header, received commands, the acknowledge and event builders, triggers, heartbeat and connection test.

4.1 Register interface

- AXI4-Lite slave, 32-bit data, 12-bit byte address: a 4 KB window. Offsets are byte offsets from the base address assigned in the Vivado address editor.
- Access types: RO read-only, RW read/write, WO write-only, WP write pulses an action, W1C write 1 to clear, W1S write 1 to set, RC counter that takes any written value (write 0 to clear; reading does not clear).
- The core answers SLVERR for an access it refuses. Reads: an offset that is not a register, `STREAM_STATUS`, `CXP_CTRL_ACK_SEND` and `CXP_EVENT_SEND`, the write-only FIFO ports, and `CXP_CTRL_RX_FIFO` while it is empty. Writes: an offset that is not a register, a read-only register, rate code 7, a connection count of 0 or above the build, a full acknowledge or event FIFO. `RST_CXP` is the one action register that reads, as 0. A register dump skips the refused reads; the supplied driver never makes them.
- The first four words (ID, VERSION, HWCFG, SCRATCH) follow the same layout in every ApotheoTech core, so one probe routine identifies any of them.

4.2 Register summary

Table 4-1. Register summary. Offsets are byte offsets from the core base address; the core decodes a 4 KB window. Offsets not listed are reserved.

OFFSET	NAME	ACCESS	FUNCTION
IDENTIFICATION AND INTERRUPTS			
0x000	ID	RO	Core identification word
0x004	VERSION	RO	Core release, major.minor.patch
0x008	HWCFG	RO	Build parameters of this instance
0x00C	SCRATCH	RW	Software scratch word
0x010	RST_CXP	WP	Reset pulses
0x014	GLBL_IER	RW	Global interrupt enable
0x018	ISR	W1C	Interrupt status, sticky
0x01C	IER	RW	Interrupt enable
0x020	IPR	RO	Interrupt pending = ISR and IER
0x024	IRQ_TEST	W1S	Set ISR bits from software
VIDEO AND CONNECTIONS			

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OFFSET	NAME	ACCESS	FUNCTION
0x028	PIXEL_TYPE	RW	Pixel format {layout, link bit depth}
0x02C	STREAM_LANES	RW	Connections that carry stream packets
0x030	VIDEO_CAP	RO	Video bus of this build
LINK STATUS AND CONTROL			
0x050	CXP_STATUS	RO	Transmitter, uplink lock, FIFO, stream and line rate status
0x054	CXP_ERRORS_HS	W1C	High-speed error flags, sticky
0x058	CXP_ERRORS_LS	W1C	Low-speed error flags, sticky
0x05C	CXP_TIMEOUTS	W1C	Acknowledge timeouts
0x060	CXP_RATE_TRANS	RW	Line rate change request
0x068	CXP_STREAM_PCKT_MAX	RW	Largest stream packet in bytes
0x080	CXP_LS_MODE	RW	CoaXPress 2.x mode
0x0B0	CXP_TX_MSTR_ID	RW	Host connection ID
IMAGE HEADER AND STREAM			
0x0B8	CXP_IMG_XSIZE	RW	Image width in pixels (Xsize)
0x0BC	CXP_IMG_XOFFS	RW	Image header Xoffs
0x0C0	CXP_IMG_YSIZE	RW	Image height in lines (Ysize)
0x0C4	CXP_IMG_YOFFS	RW	Image header Yoffs
0x0C8	CXP_IMG_BPP	RW	Bits per pixel on the link
0x0CC	CXP_RECT_PIXELF	RW	Image header PixelF
0x0D0	CXP_RECT_TAPG	RW	Image header TapG
0x0D4	CXP_RECT_FLAGS	RW	Image header flags
0x0D8	STREAM_STATUS	WP	Stream on and off
0x0DC	ACK_TIMEOUT	RW	Acknowledge timeout
RECEIVED CONTROL COMMANDS			
0x084	CXP_CTRL_RX_ERR	RO	Error flags of the last control command
0x088	CXP_CTRL_RX_CMD	RO	Last control command and size
0x08C	CXP_CTRL_RX_ADDR	RO	Last control command: address
0x090	CXP_CTRL_RX_TAG	RO	Last control command: tag
0x094	CXP_CTRL_RX_FIFO	RO	Write data of the last control command
0x11C	LS_RX_CNTRL_CRC_ERRS	RC	Control commands received with a CRC error

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OFFSET	NAME	ACCESS	FUNCTION
ACKNOWLEDGES AND EVENTS			
0x098	CXP_EVENT_ACK	RO	Last event acknowledge from the Host
0x0E0	CXP_CTRL_ACK_SEND	WP	Send the acknowledge
0x0E4	CXP_CTRL_ACK_ERRS	RO	Reserved, reads 0
0x0E8	CXP_CTRL_ACK_CODE	RW	Acknowledge code
0x0EC	CXP_CTRL_ACK_SIZE	RW	Acknowledge data size in bytes
0x0F0	CXP_CTRL_ACK_TAG	RW	Acknowledge tag
0x0F4	CXP_CTRL_ACK_FIFO	WO	Acknowledge data FIFO
0x0F8	CXP_EVENT_SEND	WP	Send the event packet
0x0FC	CXP_EVENT_TAG	RW	Event packet tag
0x100	CXP_EVENT_SIZE	RW	Event size in words
0x104	CXP_EVENT_FIFO	WO	Event data FIFO
TRIGGERS AND HEARTBEAT			
0x0A4	CXP_LS_RX_TRIG	RO	Last uplink trigger
0x0B4	CXP_TRIG_SEND	RW	Triggers to the Host
0x108	CXP_HRTBT_TIME_REG0	RW	Device time [31:0], ns
0x10C	CXP_HRTBT_TIME_REG1	RW	Device time [63:32], ns
0x110	CXP_HRTBT_CNTR_INCR	RW	Time step per aclk cycle
CONNECTION TEST			
0x09C	CXP_TEST_PCKTS_RX_CORR	RC	Good test packets received on the uplink
0x0A0	CXP_TEST_PCKTS_RX_ERR	RC	Bad test packets received on the uplink
0x114	CXP_TEST_PCKT_MODE	RW	Send test packets
0x118	CXP_TEST_PCKT_SENT	RC	Test packets sent on the downlink

Read-only Read/write Write pulse, action Write 1 to clear Reserved

4.3 Identification and interrupts

Read ID and VERSION before any write: they confirm the base address and the release. HWCFG and VIDEO_CAP tell firmware how the core was built.

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0x000 ID RO

reset 0xA71C0A02

Fixed identification word. Software reads it first: it proves that the base address points at this core.



BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:20]	VENDOR	RO	0xA71	Vendor code: 0xA71 = ApotheoTech.
[19:8]	CORE	RO	0xC0A	Core code: 0xC0A = CoaXPress.
[7:0]	FUNCTION	RO	0x02	Function: 0x02 = Device.

0x004 VERSION RO

reset 0x02020000

Release of the core in the bitstream. A new major number means another register map; a new minor number is a compatible addition; a patch has no software-visible change.



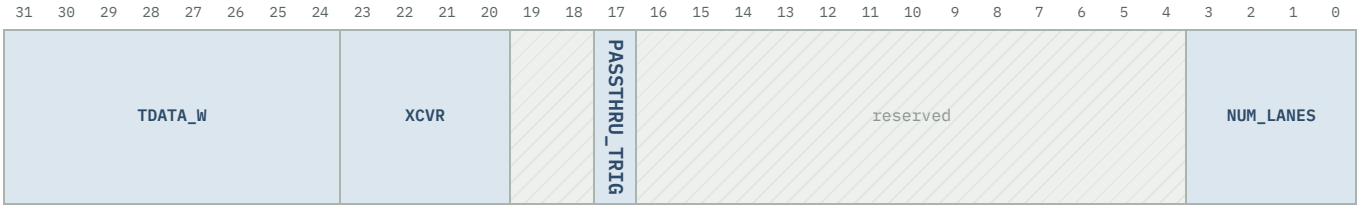
BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:24]	MAJOR	RO	0x02	Major version: register map generation.
[23:16]	MINOR	RO	0x02	Minor version.
[15:0]	PATCH	RO	0x0000	Patch level.

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0x008 HWCFG RO

reset build

The generics the core was built with, so one firmware serves every build.



BITS	FIELD	ACCESS	DESCRIPTION
[31:24]	TDATA_W	RO	`video_in` tdata width in bits.
[23:20]	XCVR	RO	Transceiver: 0 GTH (GTHE4), 1 GTY (GTYE4), 2 GTH transmitter only.
[19:18]	reserved		Reserved.
[17]	PASSTHRU_TRIG	RO	1 = the core acknowledges uplink triggers itself.
[16:4]	reserved		Reserved.
[3:0]	NUM_LANES	RO	Connections built.

0x00C SCRATCH RW

reset 0x00000000

Reads back what was written, byte strobes honoured. No effect on the core.



BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:0]	SCRATCH	RW	0	Any value.

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0x010 RST_CXP WP

Writing a 1 pulses the matching reset, so firmware can recover one path without disturbing the others. Reads 0.



BITS	FIELD	ACCESS	DESCRIPTION
[31]	ALL	WP	Reset the whole core.
[30:8]	reserved		Reserved.
[7]	LS_ALL	WP	All low-speed (uplink) logic.
[6]	HS_ALL	WP	All high-speed (downlink) logic.
[5]	HRTBT	WP	Heartbeat generator.
[4]	EVENT	WP	Event path.
[3]	CTRL_ACK	WP	Control acknowledge path.
[2]	STREAM	WP	Stream path.
[1]	CTRL_RX	WP	Control command receiver.
[0]	LS_RELOCK	WP	Re-lock the uplink receiver.

0x014 GLBL_IER RW

reset 0x00000000

Bit 0 enables the interrupt output `cxp_dev_int`.



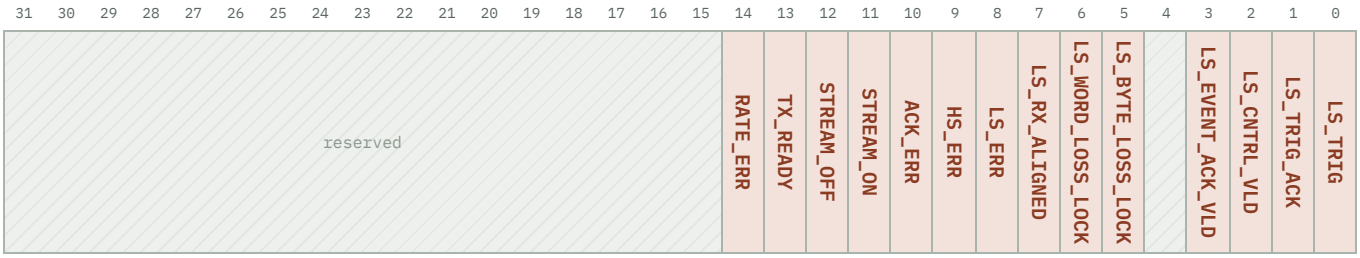
BITS	FIELD	ACCESS	DESCRIPTION
[31:1]	reserved		Reserved.
[0]	GIE	RW	1 = `cxp_dev_int` may assert.

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0x018 ISR W1C

reset 0x00000000

One sticky bit per source, set by the core whether or not the source is enabled. Write 1 to clear. A source that fires in the clock it is cleared is kept.



BITS	FIELD	ACCESS	DESCRIPTION
[31:15]	reserved		Reserved.
[14]	RATE_ERR	W1C	Line rate change failed, code in CXP_STATUS[15:14].
[13]	TX_READY	W1C	Transmitter out of reset.
[12]	STREAM_OFF	W1C	Stream stopped.
[11]	STREAM_ON	W1C	Stream started.
[10]	ACK_ERR	W1C	A CXP_TIMEOUTS flag was set.
[9]	HS_ERR	W1C	A CXP_ERRORS_HS flag was set.
[8]	LS_ERR	W1C	A CXP_ERRORS_LS flag was set.
[7]	LS_RX_ALIGNED	W1C	Uplink receiver locked: a Host is there.
[6]	LS_WORD_LOSS_LOCK	W1C	Uplink receiver lost word lock.
[5]	LS_BYTE_LOSS_LOCK	W1C	Uplink receiver lost byte lock.
[4]	reserved		Reserved.
[3]	LS_EVENT_ACK_VLD	W1C	Event acknowledge received.
[2]	LS_CNTRL_VLD	W1C	Control command received.
[1]	LS_TRIG_ACK	W1C	Trigger acknowledge received.
[0]	LS_TRIG	W1C	Trigger received on the uplink.

Table 4-2. Interrupt registers. IER, IPR and IRQ_TEST use the ISR bit positions.

OFFSET	NAME	ACCESS	MEANING
0x01C	IER	RW	One enable bit per ISR bit, same positions.
0x020	IPR	RO	The sources that drive the interrupt output now.
0x024	IRQ_TEST	W1S	Write 1 to set the matching ISR bit, to test the interrupt handler without the link.

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4.4 Video and connections

0x028 PIXEL_TYPE RW

reset generic

Pixel format of the video on `video_in`: the layout and the bit depth on the link. A write restarts the pixel packagers, so write it with the acquisition stopped. Resets to `PIXEL_TYPE_DEFAULT`.



BITS	FIELD	ACCESS	DESCRIPTION
[31:18]	reserved		Reserved.
[17]	NOT_BUILT	RO	1 = the code has no path in this bitstream. No video moves until a code that is built is written.
[16:8]	reserved		Reserved.
[7:4]	LAYOUT	RW	0 Mono / Bayer, 1 RGB, 2 YCbCr 4:4:4, 3 YCbCr 4:2:2, 4 YCbCr 4:2:0.
[3:0]	WIDTH	RW	Bit depth on the link: 8 = 8-bit, 9 = 10-bit, A = 12-bit, B = 14-bit, C = 16-bit.

0x030 VIDEO_CAP RO

reset build

What the bitstream was built with, so software can offer only the formats that exist. The default build (4 pixels per beat, 16-bit, Mono / Bayer, every bit depth) reads 0x1F011014.



BITS	FIELD	ACCESS	DESCRIPTION
[31:29]	reserved		Reserved.
[28:24]	WIDTHS	RO	Link bit depths built, bit 24 + (WIDTH - 8): 8, 10, 12, 14, 16-bit.
[23:21]	reserved		Reserved.
[20:16]	LAYOUTS	RO	Layouts built, bit 16 + LAYOUT: Mono / Bayer, RGB, YCbCr 4:4:4, 4:2:2, 4:2:0.
[15:13]	reserved		Reserved.
[12:8]	BPC	RO	VID_BPC, bits per component on the bus.
[7:4]	CPP	RO	VID_CPP, components per pixel the bus has room for.
[3:0]	PPC	RO	VID_PPC, pixels per beat.

Table 4-3. Connection register.

OFFSET	NAME	ACCESS	MEANING

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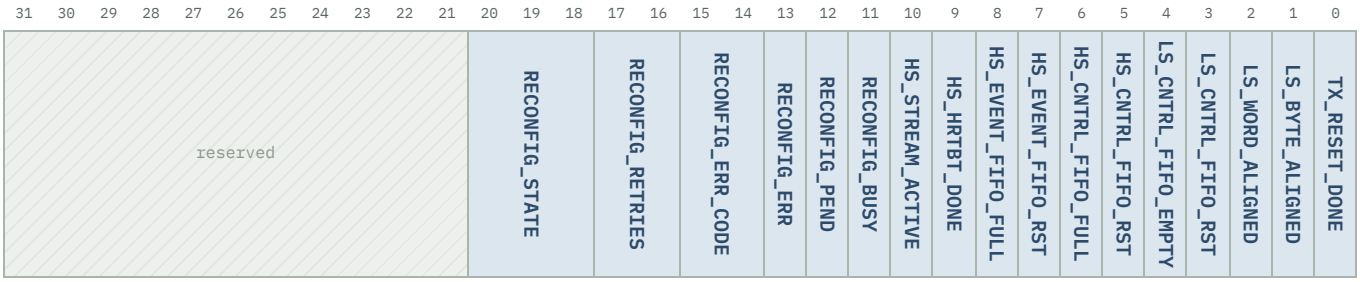
OFFSET	NAME	ACCESS	MEANING
0x02C	STREAM_LANES	RW	Bits [2:0]: 1 to NUM_LANES. Every write resets the stream control: packet tag 0, first packet on connection 0. Write it on ConnectionConfig and after a ConnectionReset. 0, or more connections than the build has, is refused with SLVERR.

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4.5 Link status and control

0x050 CXP_STATUS RO

Live status of the core. Bits [20:11] describe the last line rate request and are laid out the same in the Host and the Device core.

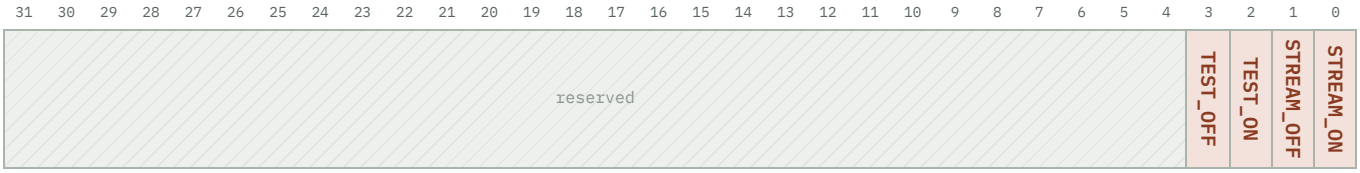


BITS	FIELD	ACCESS	DESCRIPTION
[31:21]	reserved		Reserved.
[20:18]	RECONFIG_STATE	RO	Line rate change state: 0 idle, 1 DRP writes, 2 reset held, 3 waiting for the reset to be taken, 4 waiting for reset done.
[17:16]	RECONFIG_RETRIES	RO	Extra PLL resets the last request needed.
[15:14]	RECONFIG_ERR_CODE	RO	Error of the last request: 1 DRP no answer, 2 reset not acknowledged, 3 transmitter reset done never back.
[13]	RECONFIG_ERR	RO	The last request failed.
[12]	RECONFIG_PEND	RO	A request is latched and not yet launched.
[11]	RECONFIG_BUSY	RO	A line rate change is running.
[10]	HS_STREAM_ACTIVE	RO	The stream is on.
[9]	HS_HRTBT_DONE	RO	Heartbeat generator idle.
[8]	HS_EVENT_FIFO_FULL	RO	Event FIFO full.
[7]	HS_EVENT_FIFO_RST	RO	Event FIFO in reset.
[6]	HS_CNTRL_FIFO_FULL	RO	Acknowledge FIFO full.
[5]	HS_CNTRL_FIFO_RST	RO	Acknowledge FIFO in reset.
[4]	LS_CNTRL_FIFO_EMPTY	RO	Received command FIFO empty.
[3]	LS_CNTRL_FIFO_RST	RO	Received command FIFO in reset.
[2]	LS_WORD_ALIGNED	RO	Uplink receiver word aligned: a Host is there.
[1]	LS_BYTE_ALIGNED	RO	Uplink receiver byte aligned.
[0]	TX_RESET_DONE	RO	Transmitter reset done.

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0x05C CXP_TIMEOUTS W1C

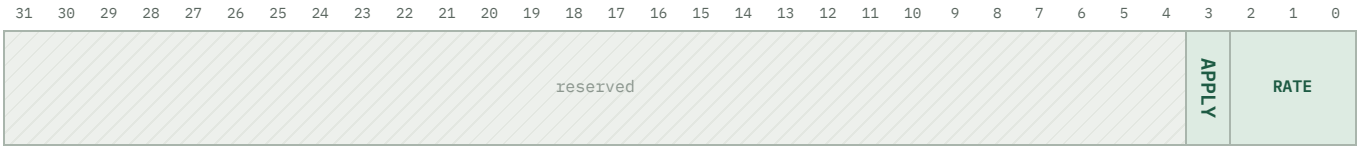
Set when the stream or the test path does not confirm an on or off request within ACK_TIMEOUT. Any flag raises ACK_ERR.



BITS	FIELD	ACCESS	DESCRIPTION
[31:4]	reserved		Reserved.
[3]	TEST_OFF	W1C	Test packets off not confirmed.
[2]	TEST_ON	W1C	Test packets on not confirmed.
[1]	STREAM_OFF	W1C	Stream off not confirmed.
[0]	STREAM_ON	W1C	Stream on not confirmed.

0x060 CXP_RATE_TRANS RW

Writing bit 3 = 1 starts a line rate change to the speed in bits [2:0]: the core rewrites the transceiver PLL and dividers over DRP, resets the PLL and datapath, and waits for the transceiver to come back. A request that arrives while one runs is kept (newest wins) and runs next. Progress and errors are in `CXP_STATUS[20:11]`; the RATE_DONE and RATE_ERR interrupts report the end. The Device refuses rate code 7 with SLVERR.

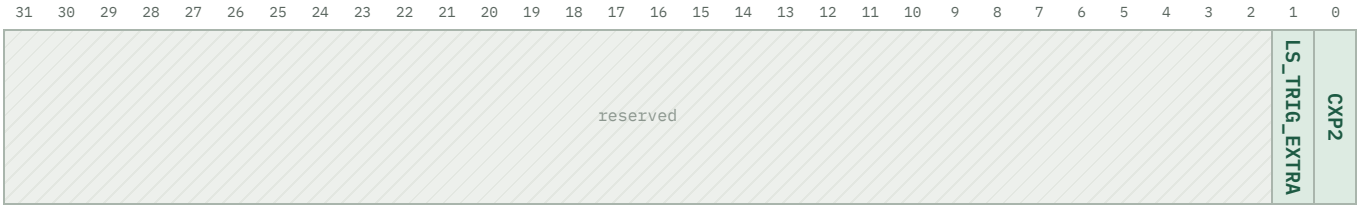


BITS	FIELD	ACCESS	DESCRIPTION
[31:4]	reserved		Reserved.
[3]	APPLY	RW	1 = start the rate change.
[2:0]	RATE	RW	Line rate code, CXP-1 to CXP-12. The supplied driver holds the code table.

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0x080 CXP_LS_MODE RW

Bit 0: CXP 2.x operation (tagged commands, heartbeat). Bit 1: extra low-speed trigger.



BITS	FIELD	ACCESS	DESCRIPTION
[31:2]	reserved		Reserved.
[1]	LS_TRIG_EXTRA	RW	Extra low-speed trigger.
[0]	CXP2	RW	1 = CXP 2.x: tagged commands and heartbeat.

Table 4-4. Error flags, packet size and Host ID.

OFFSET	NAME	ACCESS	MEANING
0x054	CXP_ERRORS_HS	W1C	Sticky flags of the downlink packet builders, including errors in an acknowledge built by firmware (bits [6:0]). Write 1 to clear. Any flag raises HS_ERR.
0x058	CXP_ERRORS_LS	W1C	Sticky flags of the uplink receiver. Write 1 to clear. Any flag raises LS_ERR.
0x068	CXP_STREAM_PCKT_MAX	RW	StreamPacketSizeMax agreed with the Host. 0 = no stream packets.
0x0B0	CXP_TX_MSTR_ID	RW	The MasterHostConnectionID written by the Host at discovery. Goes into event and heartbeat packets.

4.6 Image header and stream

The rectangular image header fields and the stream on and off control. See Image header and stream.

Table 4-5. Image header fields and stream control. The header is taken at stream on.

OFFSET	NAME	ACCESS	MEANING
0x0B8	CXP_IMG_XSIZE	RW	Image width in pixels (Xsize).
0x0BC	CXP_IMG_XOFFS	RW	Image header Xoffs.
0x0C0	CXP_IMG_YSIZE	RW	Image height in lines (Ysize).
0x0C4	CXP_IMG_YOFFS	RW	Image header Yoffs.
0x0C8	CXP_IMG_BPP	RW	Bits per pixel on the link: 8, 10, 12, 14, 16 or 24.
0x0CC	CXP_RECT_PIXELF	RW	The CoaXPress PixelF code of the image.
0x0D0	CXP_RECT_TAPG	RW	Image header TapG.
0x0D4	CXP_RECT_FLAGS	RW	Image header flags.

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OFFSET	NAME	ACCESS	MEANING
0x0D8	STREAM_STATUS	WP	Bit 0: stream on, taking the image header registers. Bit 1: stream off. Not readable: a read is refused with SLVERR.
0x0DC	ACK_TIMEOUT	RW	aclk cycles to wait for the stream or test path to confirm an on or off request. Resets to the **Acknowledge timeout after reset** set in the IP GUI.

4.7 Received control commands

Table 4-6. The last control command received from the Host.

OFFSET	NAME	ACCESS	MEANING
0x084	CXP_CTRL_RX_ERR	RO	Error flags of the last control command.
0x088	CXP_CTRL_RX_CMD	RO	Bits [31:24]: command. Bits [23:0]: size in bytes.
0x08C	CXP_CTRL_RX_ADDR	RO	Last control command: address.
0x090	CXP_CTRL_RX_TAG	RO	Bits [7:0], CXP 2.x.
0x094	CXP_CTRL_RX_FIFO	RO	One word per read. A read of an empty FIFO is refused with SLVERR.
0x11C	LS_RX_CNTRL_CRC_ERRS	RC	Control commands received with a CRC error.

4.8 Acknowledges and events

Firmware builds an acknowledge or an event in these registers and sends it with one write.

Table 4-7. Acknowledge and event builders.

OFFSET	NAME	ACCESS	MEANING
0x098	CXP_EVENT_ACK	RO	Bits [7:0]: tag.
0x0E0	CXP_CTRL_ACK_SEND	WP	Bit 0 sends the control acknowledge built from the code, size, tag and data registers. Not readable.
0x0E4	CXP_CTRL_ACK_ERRS	RO	Reserved, reads 0. Errors of an acknowledge built by firmware are in CXP_ERRORS_HS[6:0].
0x0E8	CXP_CTRL_ACK_CODE	RW	Bits [7:0].
0x0EC	CXP_CTRL_ACK_SIZE	RW	Acknowledge data size in bytes.
0x0F0	CXP_CTRL_ACK_TAG	RW	Bits [7:0]: the tag received with the command.
0x0F4	CXP_CTRL_ACK_FIFO	WO	One word per write. A write to a full FIFO is refused with SLVERR.
0x0F8	CXP_EVENT_SEND	WP	Bit 0 sends the event built from the tag, size and data registers. Not readable.
0x0FC	CXP_EVENT_TAG	RW	Bits [7:0].
0x100	CXP_EVENT_SIZE	RW	Event size in words.

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OFFSET	NAME	ACCESS	MEANING
0x104	CXP_EVENT_FIFO	WO	One word per write. A write to a full FIFO is refused with SLVERR.

4.9 Triggers and heartbeat

0x0B4 CXP_TRIG_SEND RW

Bits [7:0]: trigger indication. Bit 8: send a high-speed trigger. Bit 9: send a trigger acknowledge.



BITS	FIELD	ACCESS	DESCRIPTION
[31:10]	reserved		Reserved.
[9]	SEND_ACK	RW	Send a trigger acknowledge.
[8]	SEND_TRIG	RW	Send a high-speed trigger.
[7:0]	INDICATION	RW	Trigger indication carried by the trigger.

Table 4-8. Trigger and heartbeat registers.

OFFSET	NAME	ACCESS	MEANING
0x0A4	CXP_LS_RX_TRIG	RO	Trigger number and delay of the last trigger received from the Host.
0x108	CXP_HRTBT_TIME_REG0	RW	Low word of the Device time sent in every heartbeat.
0x10C	CXP_HRTBT_TIME_REG1	RW	Device time [63:32], ns.
0x110	CXP_HRTBT_CNTR_INCR	RW	Nanoseconds added to the Device time every aclk cycle.

4.10 Connection test

Table 4-9. Connection test registers.

OFFSET	NAME	ACCESS	MEANING
0x09C	CXP_TEST_PCKTS_RX_CORR	RC	Good test packets received on the uplink.
0x0A0	CXP_TEST_PCKTS_RX_ERR	RC	Bad test packets received on the uplink.
0x114	CXP_TEST_PCKT_MODE	RW	Bit 0: send test packets on the downlink (TestMode).
0x118	CXP_TEST_PCKT_SENT	RC	Test packets sent on the downlink.

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4.11 Camera bring-up sequence

What the firmware does from power-up to streaming, in register terms. The frame grabber drives discovery; the camera answers.

01 Identify the core

Read `ID` (expect 0xA71C0A02) and `VERSION` (0x02020000 for v2.2.0). Read `HWCFG` and `VIDEO_CAP`.

02 Interrupts

Clear `ISR`, enable LS_CNTRL_VLD, LS_RX_ALIGNED, the loss of lock sources, STREAM_ON, STREAM_OFF, TX_READY and RATE_ERR in `IER`, set `GLBL_IER`.

03 Wait for a Host

LS_RX_ALIGNED fires when a frame grabber is on the line. Commands arrive with LS_CNTRL_VLD.

04 Serve the control channel

For every command, read it from the received command registers, act on the camera's register space, and answer through the acknowledge builder. On a write to MasterHostConnectionID, write the ID to `CXP_TX_MSTR_ID`; on CXP 2.x set `CXP_LS_MODE` bit 0.

05 Change speed

On ConnectionConfig, acknowledge first, then write `CXP_RATE_TRANS` with the new speed and `APPLY`, and `STREAM_LANES`. TX_READY reports the transmitter back at the new speed.

06 Start the stream

On AcquisitionStart, write the image header registers, `PIXEL_TYPE` and `CXP_STREAM_PCKT_MAX`, then `STREAM_STATUS` bit 0. STREAM_ON confirms it.

07 Stop the stream

On AcquisitionStop, write `STREAM_STATUS` bit 1. STREAM_OFF fires when the frame in flight has gone out.

The first accesses with plain register reads and writes:

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```
/* base = address of cxp_dev_0 in the Vivado address editor */
#define DEV(off)  (base + (off))

if (Xil_In32(DEV(0x000)) != 0xA71C0A02) return -1;    /* ID               */
u32 ver = Xil_In32(DEV(0x004));                          /* VERSION 2.2.0     */

Xil_Out32(DEV(0x018), 0xFFFFFFFF);   /* ISR: clear everything           */
Xil_Out32(DEV(0x01C), 0x78E4);       /* IER: CNTRL_VLD, lock, STREAM_ON, */
                                        /*      STREAM_OFF, TX_READY, RATE_ERR */
Xil_Out32(DEV(0x014), 1);            /* GLBL_IER                        */

/* AcquisitionStart: header, format, packet size, then stream on */
Xil_Out32(DEV(0x0B8), 3840);         /* CXP_IMG_XSIZE                   */
Xil_Out32(DEV(0x0C0), 2160);         /* CXP_IMG_YSIZE                   */
Xil_Out32(DEV(0x028), 0x08);         /* PIXEL_TYPE: Bayer 8-bit         */
Xil_Out32(DEV(0x0D8), 1);            /* STREAM_STATUS: stream on        */
```

The firmware driver supplied with the core performs these steps and the command loop; see Software.

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SECTION 05

Example Designs and Software

The APT-C11-FMC CoaXPress card, the basic camera and DisplayPort loopback designs, the bring-up flow and the firmware that comes with the core.

5.1 Evaluation hardware

The **APT-C11-FMC** is ApotheoTech's CoaXPress FMC card, built for the Host and Device cores: coax connectors, CoaXPress cable drivers, equalizers and uplink circuits, wired to the transceivers of the carrier board. A ZCU106 with the card is a CoaXPress camera any frame grabber can talk to.

Table 5-1. Evaluation platforms.

BOARD	DEVICE	TRANSCEIVER	EXAMPLE DESIGNS
AMD ZCU106 + APT-C11-FMC	Zynq UltraScale+ MPSoC XCZU7EV	GTH	Basic camera; DisplayPort loopback, demo bitstream
Your board	Any supported AMD device	GTH, GTH TX only, GTY	Custom integration (NRE)

5.2 Demo bitstream

A free demo bitstream for the ZCU106 with the APT-C11-FMC runs the Device and the Host core in loopback and shows the received video on a DisplayPort monitor: the standard test of the cores, with discovery, the line rate change and the pixel formats running before you build anything.

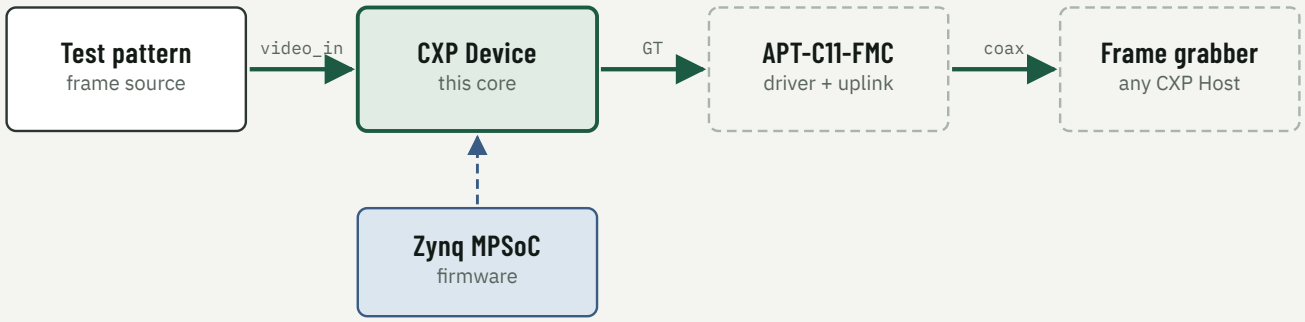
5.3 Example designs

Each example design is a complete Vivado project: the block design, constraints, a script that recreates the project, the transceiver wrapper and the firmware.

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Basic camera

Included

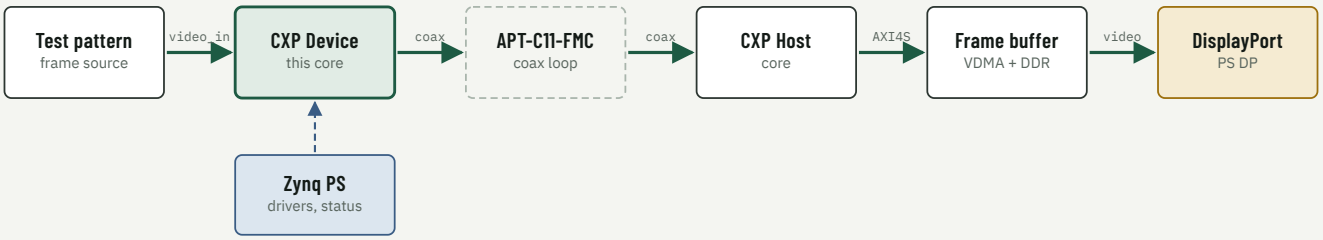


A test pattern generator feeds the Device core, and the Zynq MPSoC runs the camera firmware: the command loop, the bootstrap registers, the line rate change and stream on and off. Plug it into any CoaXPress 2.1 frame grabber. The starting point for a camera: replace the test pattern with your image pipeline.

Core Device **Platform** ZCU106 + APT-C11-FMC **Firmware** bare-metal on the Arm cores

DisplayPort loopback

Included with Host + Device



The Device and the Host core over coax through the APT-C11-FMC on one board, with the received video on the DisplayPort output of the Zynq MPSoC. Free to anyone who licenses both cores.

Cores Device and Host **Platform** ZCU106 + APT-C11-FMC **Software** bare-metal, DisplayPort

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Custom integration

NRE

Work directly with ApotheoTech on your camera: your sensor and board, an SLVS-EC sensor through the ApotheoTech SLVS-EC Receiver on the same transceiver quad, an ISP in front of the core, 2 and 4 connection links, or a complete camera with its GenICam description.

5.4 Bring-up flow

01 Recreate the project
Run the example design's Tcl script in Vivado. It adds the IP repository, builds the block design and applies the constraints.

02 Choose the build
In the IP GUI pick the transceiver option, set the AXI4-Lite clock, switch on the pixel layouts and bit depths your camera sends, and set pixels per beat and bits per component to match your video source.

03 Build and export
Generate the bitstream and export the hardware platform for Vitis.

04 Build the firmware
Create the Vitis platform and application, add the example sources and the driver.

05 Run
Program the board and connect a frame grabber. The console prints the core version and build, and each discovery step as the grabber runs it.

06 Stream
Start acquisition from the frame grabber's software. The test pattern appears at the operating speed.

5.5 Software

The core comes with a firmware driver for setup and control, supplied on purchase, for MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC processors. It identifies the core and its build, services the interrupts, receives control commands and sends acknowledges, sends events, runs the line rate change, starts and stops the stream, and reads the status. The example designs use it, and the basic camera adds a working command loop with the CoaXPress bootstrap registers, so it doubles as the skeleton of your camera firmware.

5.6 Verification

The Device core is verified against the ApotheoTech Host core over a model of the link, and on its own in a UVM 1.2 testbench, with a link monitor that checks IDLE spacing and packet tags on every word.

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- Both cores back to back: identification, control reads and writes (untagged at discovery, tagged at the operating speed), interrupts, every pixel format of the build, events, heartbeat, triggers in both directions, connection test, line rate change errors with recovery, CRC error injection and stalls on every FIFO.
- The pixel path is checked for 11 bus builds and every format each carries, up to 25: the link words against a bit-serial model of CoaXPress 2.1, built from the pixels, and the beats through the Host against the UG934 beat.
- The line rate change is checked against a transceiver model for every failure: DRP not answering, reset not connected, PLL never locking, a request during a change, and a reset during a change.
- The stream stop is checked with the source running and with the source already quiet.

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SECTION 06

Resources and Ordering

Device support, what each pixel format costs, the licensing configurations, what you receive and how to evaluate and order.

6.1 Supported devices

Table 6-1. AMD device and transceiver support.

FAMILY	TRANSCEIVER	SPEEDS	STATUS
Zynq UltraScale+ MPSoC, including Kria K26	GTH (GTHE4), GTH transmitter only	CXP-1 to CXP-12	Example designs
Kintex UltraScale+	GTY (GTYE4), GTH (GTHE4)	CXP-1 to CXP-12	Contact ApotheoTech
Other UltraScale+ devices	GTH, GTY	CXP-1 to CXP-12	Contact ApotheoTech
7 series and other families	Per family		NRE engagement

6.2 Resource utilization

The pixel formats you switch on set most of the size difference between builds. The table below is an estimate of the pixel path block alone, so you can see what a format costs; read it as one build against another. A Vivado utilization report for your build, including the transmit path, the protocol handling and the FIFOs, comes with the evaluation.

Table 6-2. What a format switch costs: estimate of the pixel path block alone at 4 pixels of 16 bits per beat, UltraScale+. Read it as the size of one build against another; it is not a Vivado utilization report.

FORMATS BUILT	HOST LUT	HOST FF	DEVICE LUT	DEVICE FF	DEVICE BRAM
Mono / Bayer, 8-bit only	127	86	98	91	
Mono / Bayer, 8, 10 and 12-bit	406	275	413	289	
Mono / Bayer, every depth (default)	841	510	792	489	
adds YCbCr 4:2:2	1,051	707	883	625	
adds YCbCr 4:2:2 and 4:2:0	1,089	708	933	701	2
adds RGB	1,194	836	921	690	
adds RGB and YCbCr 4:4:4	1,263	836	1,160	690	
everything (25 formats)	1,389	1,034	1,207	902	2

- Bit depths are the larger lever: each depth in **Bit depths on the link** is a gearbox of its own. A product that only runs 8 to 12-bit saves about half of the pixel path.
- RGB and YCbCr 4:4:4 share one layout block, YCbCr 4:2:2 and 4:2:0 the other; switching off one of a pair saves little.

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- The video input FIFO is `tdata` + 2 bits wide: one BRAM36 at 512 beats of the default 64-bit bus, three for the 192-bit bus. YCbCr 4:2:0 adds the chroma line store, two BRAM36 at 4,096 pixels.

6.3 Licensing configurations

Table 6-3. The CoaXPress cores are licensed in four configurations.

CONFIGURATION	CONTENTS	FOR
Host Only	CoaXPress 2.1 Host core	Frame grabbers and embedded vision systems that take any CoaXPress camera
Host + Test Device	Host core and a Device core restricted to its internal test pattern, without a video input	Capture card developers who need a link partner for test and production
Device Only	CoaXPress 2.1 Device core	Camera makers
Host + Device	Both cores; includes the DisplayPort loopback example design	Complete camera-to-grabber systems and bridges

6.4 Deliverables

Table 6-4. What a license includes.

IP core	Encrypted netlist for the target FPGA family and transceiver, packaged for Vivado IP Integrator with its customization GUI
Transceiver wrapper	GTH or GTY transceiver wrapper set up for CoaXPress, with the line rate tables the core uses
Integration guide	Interface descriptions, register map, integration checklist
Instantiation templates	Verilog and VHDL wrapper templates
Example designs	Complete Vivado projects for the licensed configuration
Software	Driver for setup and control on MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC, plus the example applications
Updates and support	One year of updates and email support included; renewal afterwards

6.5 Evaluation and ordering

Evaluate

The free ZCU106 demo bitstream runs Host and Device in loopback with the APT-C11-FMC. Ask for an evaluation of your build.

License

Perpetual license with one year of updates. Add-on example designs and NRE engineering on request.

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Engineering services

Integration on your board, sensor front ends and ISP pipelines, 2 and 4 connection builds, complete CoaXPress cameras.

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Web: apotheotech.com

For pricing, evaluation access or technical questions, email us with your sensor, speed, pixel formats and target device.

Related ApotheoTech products: the CoaXPress 2.1 Host IP core, the SLVS-EC Receiver IP core, the APT-C11-FMC CoaXPress card and the Aper-Oculus Kria K26 carrier board.

6.6 Revision history

Table 6-5. Datasheet revisions.

REVISION	DATE	CHANGES
1.0	November 2026	First release, for IP v2.2.0.

6.7 Notices

CoaXPress is a trademark of the Japan Industrial Imaging Association (JIIA). JIIA CXP-001-2021 is published by the JIIA. GenICam is a trademark of the European Machine Vision Association (EMVA). AMD, Xilinx, Zynq, Kria, Kintex, UltraScale, Vivado and Vitis are trademarks of Advanced Micro Devices, Inc. All other names are the property of their respective owners. Specifications are subject to change without notice. This document describes the IP core and does not grant any license.