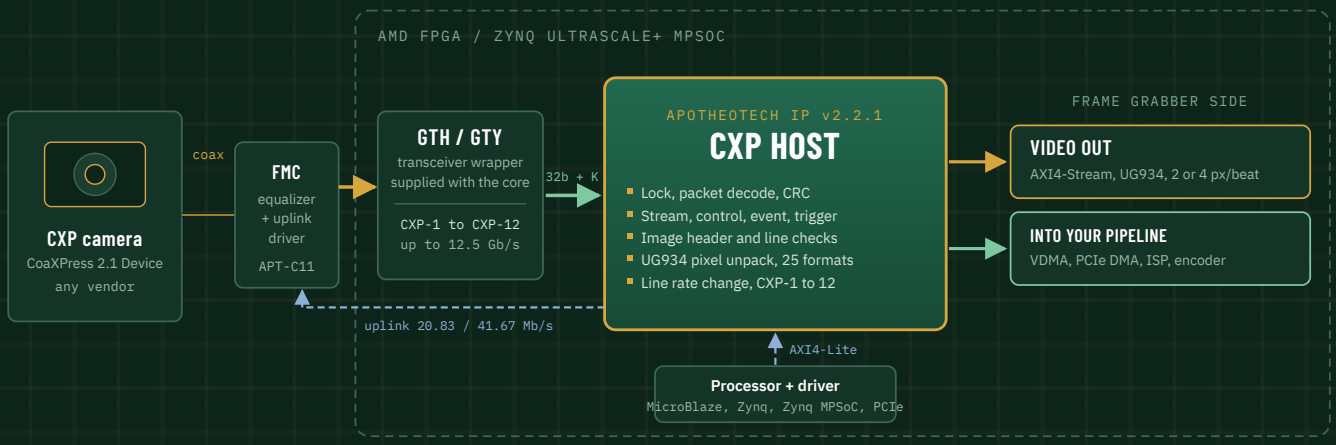
APOTHEOTECH

IP CORE DATASHEET
APT-DS-CXP-HOST-0001
Rev 1.0 · IP v2.2.1
November 2026

COAXPRESS 2.1 FRAME GRABBER CORE FOR AMD FPGAS

CoaXPress 2.1 Host IP Core

Receives a CoaXPress camera at CXP-1 to CXP-12 on GTH or GTY transceivers and delivers frames as UG934 AXI4-Stream video in up to 25 pixel formats, with the control channel, events, triggers, heartbeat and line rate change handled in hardware.



12.5 Gb/s
per connection, CXP-12

25
pixel formats, built by switch

Mono to YCbCr
8 to 16-bit

GTH or GTY
transceiver wrapper supplied

info@apotheotech.com

CONTENTS

Contents

01 Overview

1.1 Introduction
1.2 Features
1.3 Key specifications
1.4 Throughput
1.5 Applications

02 Functional Description

2.1 Architecture
2.2 Transceiver and link
2.3 Packet handling
2.4 Video bus
2.5 Pixel formats
2.6 Control channel
2.7 Events, triggers and heartbeat
2.8 Line rate change
2.9 Interrupts
2.10 Buffering and overflow
2.11 Clocks and reset

03 Interfaces and Timing

3.1 IP customization parameters
3.2 Interface overview
3.3 Interface descriptions
3.4 Video output timing
3.5 Integration checklist

04 Register Map

4.1 Register interface
4.2 Register summary
4.3 Identification and interrupts
4.4 Video and connections
4.5 Link status and control
4.6 Control channel
4.7 Events, triggers and heartbeat
4.8 Stream and image header
4.9 Connection test
4.10 Error counters
4.11 Statistics
4.12 Link bring-up sequence

05 Example Designs and Software

5.1 Evaluation hardware
5.2 Demo bitstream
5.3 Example designs
5.4 Bring-up flow
5.5 Software
5.6 Verification

06 Resources and Ordering

6.1 Supported devices
6.2 Resource utilization
6.3 Licensing configurations
6.4 Deliverables
6.5 Evaluation and ordering
6.6 Revision history
6.7 Notices

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 01

Overview

A CoaXPress 2.1 Host link layer for AMD FPGAs, from the coax to UG934 AXI4-Stream video.

1.1 Introduction

The ApotheoTech CoaXPress 2.1 Host IP Core implements the Host link layer of the JIIA CXP-001-2021 CoaXPress standard, version 2.1: the side of the link that sits in a frame grabber or an embedded vision system and takes video from a camera. It runs on the GTH or GTY transceivers of AMD UltraScale+ devices through a transceiver wrapper supplied with the core, and drives the low-speed uplink to the camera.

The core locks to the camera, checks every packet, and sorts what arrives: stream packets go through the image header parser and the pixel path to an AXI4-Stream video master on your clock; control acknowledges, events, heartbeats and triggers go to registers, FIFOs and interrupts for software. On the uplink it sends control commands, triggers, event acknowledges and test packets. A line rate change is a single register write: the core rewrites the transceiver over DRP, resets it and reports the result.

The video output follows AMD UG934, so it connects to AMD video IP, a frame buffer writer, a PCIe DMA or your own pipeline without an adapter. The bus width and the set of pixel formats are chosen in the IP GUI, so a build carries only the formats your product uses.

1.2 Features

LINK LAYER

- CoaXPress 2.1 Host (JIIA CXP-001-2021), with untagged commands for discovery
- CXP-1 to CXP-12: 1.25 to 12.5 Gb/s on one connection
- Low-speed uplink at 20.83 Mb/s, and 41.67 Mb/s for CXP-10 and CXP-12
- Lock on IDLE words, packet framing and CRC check on every packet
- Line rate change in hardware: DRP rewrite, PLL reset, retries and an error code
- GTH (GTHE4) or GTY (GTYE4) transceiver, wrapper supplied with the core

PROTOCOL

- Control channel: read and write commands, tagged (CXP 2.x) or untagged, acknowledge FIFO
- Event packets into a FIFO, acknowledged by software or by the core
- High-speed triggers from the camera, acknowledged by the core or by software; triggers to the camera on the uplink
- Heartbeat with the camera’s time stamp and Host ID check
- Connection test packets in both directions with counters
- Image header and line markers parsed, line and frame size checked against the header

VIDEO OUTPUT

- UG934 AXI4-Stream video: `tuser` start of frame, `tlast` end of line, on its own clock
- 2 or 4 pixels per beat, 8 to 16 bits per component, 1 to 3 components per pixel
- Mono, Bayer and Raw; RGB; YCbCr 4:4:4, 4:2:2 and 4:2:0; 8, 10, 12, 14 and 16-bit

INTEGRATION

- AXI4-Lite control in a 4 KB window with ID, version and build discovery
- Interrupt controller with status, enable, pending and software test registers
- Word, register and video clocks fully independent; all crossings inside the core

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

- Each layout and bit depth built only when switched on in the IP GUI
- Format selected at run time by one register write, also driven on a port for the logic behind the core
- Overflow, line width and format errors counted, never passed on silently
- Packaged for Vivado IP Integrator with a customization GUI
- Software driver for setup and control on MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC
- Example designs on ZCU106 and KCU116 with the APT-C11-FMC CoaXPress card

1.3 Key specifications

Table 1-1. Key specifications of the CoaXPress 2.1 Host IP Core v2.2.1.

Standard	JIIA CXP-001-2021, CoaXPress 2.1, Host link layer
Connections	1 (one coax). Builds for 2 and 4 connections on request
Speeds	CXP-1, CXP-2, CXP-3, CXP-5, CXP-6, CXP-10, CXP-12: 1.25 to 12.5 Gb/s, changed at run time
Uplink	20.83 Mb/s; 41.67 Mb/s at CXP-10 and CXP-12
Transceiver	AMD UltraScale+ GTH (GTHE4) or GTY (GTYE4), through the supplied transceiver wrapper
Video output	AXI4-Stream, AMD UG934 video convention, on its own clock
Bus	2 or 4 pixels per beat (`VID_PPC`), 8 to 16 bits per component (`VID_BPC`), 1 to 3 components (`VID_CPP`); `tdata` 16 to 192 bits, default 64
Pixel formats	Mono / Bayer / Raw, RGB, YCbCr 4:4:4, 4:2:2, 4:2:0; 8, 10, 12, 14, 16-bit on the link; up to 25 per build
Pixel rate	Up to 1,220 Mpx/s on one CXP-12 connection (Mono 8-bit, 4 pixels per beat)
Protocol	Stream, control (tagged and untagged), events, heartbeat, triggers both directions, connection test
Error accounting	22 error counters with sticky flags, 11 statistics counters, last image header in registers
Control interface	AXI4-Lite slave, 32-bit data, 12-bit address (4 KB), 83 registers
Interrupt	`cxp_int`, 14 sources, level with a re-arm gap after each status write
Clocks	Word clock from the transceiver = line rate / 40 (312.5 MHz at CXP-12); AXI4-Lite clock 50 to 300 MHz; video clock independent
Target devices	AMD Zynq UltraScale+ MPSoC, Kria K26 SOM and Kintex UltraScale+; other UltraScale+ devices with GTH or GTY transceivers
Software	Driver for setup and control on MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC, supplied on purchase; Linux driver and application with the PCIe example design
Design flow	AMD Vivado Design Suite, IP Integrator or RTL instantiation

1.4 Throughput

The receiver keeps up with the link at every speed. The pixel path runs on the word clock and takes one 32-bit link word per clock, so at 4 pixels per beat it carries every format at the full rate of the connection. At 2 pixels per beat only Mono and Bayer formats below 16 bits leave link capacity unused.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

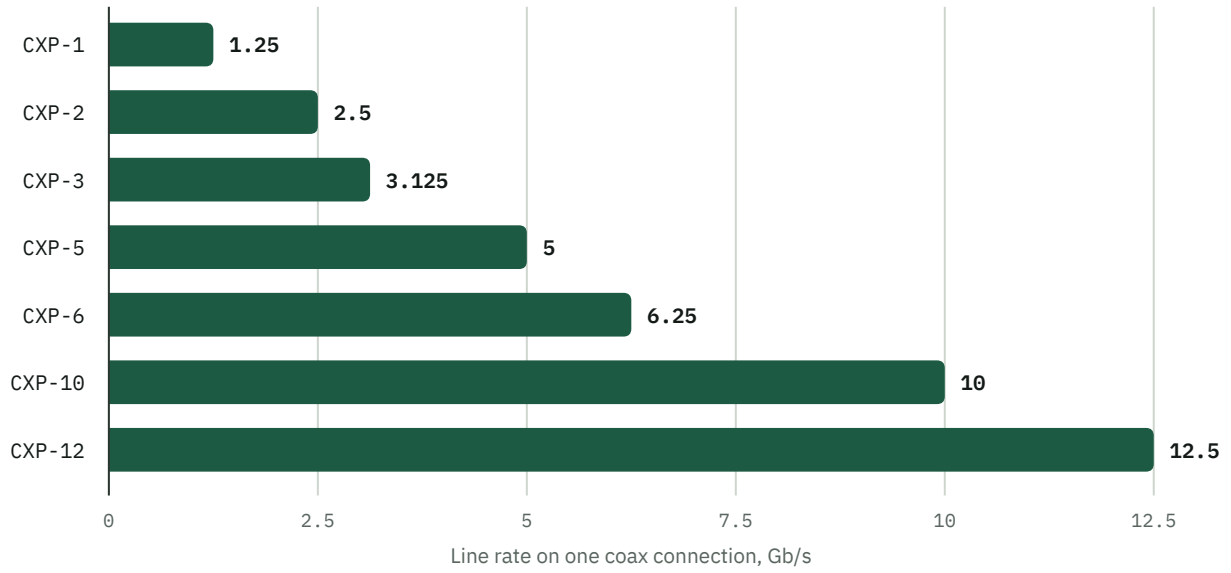


Figure 1-1. Line rate per CoaXPress speed on one connection. Hover a bar for the payload rate and the uplink rate.

Table 1-2. CoaXPress speeds on one connection. The word clock is the line rate / 40 (one 32-bit word per clock); payload is the line rate after 8b/10b decoding, before packet overhead.

SPEED	LINE RATE GB/S	PAYLOAD GB/S	PAYLOAD MB/S	WORD CLOCK MHZ	UPLINK MB/S
CXP-1	1.25	1	125.0	31.25	20.83
CXP-2	2.5	2	250.0	62.5	20.83
CXP-3	3.125	2.5	312.5	78.125	20.83
CXP-5	5	4	500.0	125	20.83
CXP-6	6.25	5	625.0	156.25	20.83
CXP-10	10	8	1,000.0	250	41.67
CXP-12	12.5	10	1,250.0	312.5	41.67

1.5 Applications

Frame grabbers
PCIe CoaXPress capture cards on Kintex and Zynq

Embedded vision
CoaXPress cameras straight into a Zynq MPSoC pipeline

Industrial inspection
High-speed area and line scan cameras

Medical imaging
Deterministic capture with full error accounting

Semiconductor metrology
High-resolution cameras at CXP-12

Defense and aerospace
Long cable runs, power and data on one coax

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

Camera test systems
Paired with the CoaXPress Device core for loopback

Video bridges
CoaXPress to PCIe, Ethernet, SDI or DisplayPort

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 02

Functional Description

How the Host core turns a CoaXPress downlink into video and software events: the receive path, the video bus and pixel formats, the control channel, events, triggers, line rate change, interrupts and clocks.

2.1 Architecture

The core is the Host link layer. The supplied transceiver wrapper recovers the clock and the 8b/10b words from the coax; the core takes 32-bit words and their K flags from there, on the word clock of the transceiver. Every packet passes the stages below. Video leaves on an AXI4-Stream on your clock; everything else is handed to software through the register file.

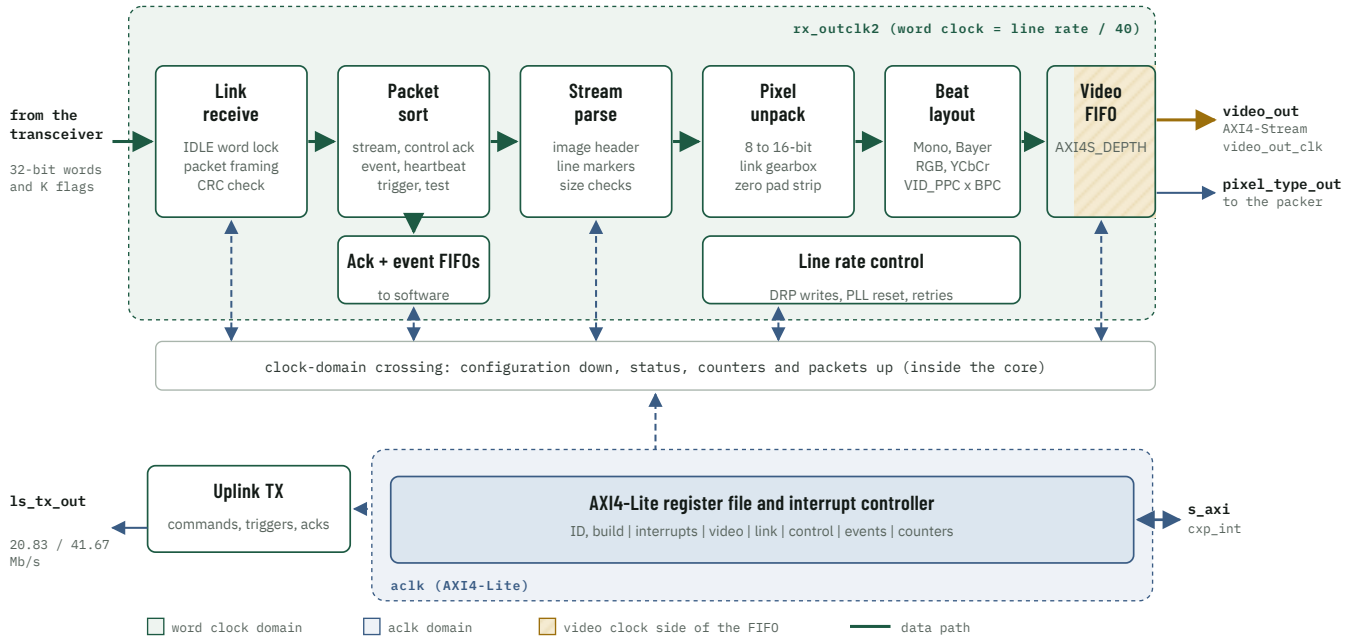


Figure 2-1. Functional block diagram. The receive path runs on the transceiver word clock; the register file and the interrupt controller run on the AXI4-Lite clock; the video FIFO is read on the video clock. All crossings are inside the core.

01 Link receive

Aligns the words on the IDLE word, declares lock after a run of good IDLE words, frames packets on their K codes and checks the CRC of every packet.

02 Packet sort

Sends stream packets to the stream path, and control acknowledges, events, heartbeats, triggers and test packets to their own handlers, FIFOs and interrupts.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

03 Stream parse
Checks stream packet tags and sizes, takes the rectangular image header and the line markers, and checks every line and frame against the header.

04 Pixel unpack
Turns the link words back into components of the selected bit depth, 8 to 16 bits, and drops the zero padding at the end of each line.

05 Beat layout
Places the components on the UG934 beat: `VID_PPC` pixels of `VID_BPC`-bit components, in the order of the selected layout.

06 Video FIFO
Crosses to the video clock and drives `video_out` with `tuser` at the start of each frame and `tlast` at the end of each line.

2.2 Transceiver and link

The core runs on an AMD UltraScale+ GTH or GTY transceiver, selected with **Transceiver** in the IP GUI. The transceiver wrapper is delivered with the core, set up for CoaXPress: line rates, 8b/10b, word alignment control and the DRP rate tables the core uses for a line rate change. The coax itself needs a CoaXPress equalizer and an uplink driver between the connector and the FPGA, as on the APT-C11-FMC.

- **Lock.** A connection is locked after 64 consecutive IDLE words by default (**IDLE words for lock**, 64 to 1,024) and counts an error when a run of words passes without an IDLE word (**Words without IDLE for an error**). `CXP_STATUS.RX_LOCKED` and the LOCKED and LOSS_LOCK interrupts report it.
- **Uplink.** The core sends on `ls_tx_out` at 20.83 Mb/s, or 41.67 Mb/s for CXP-10 and CXP-12 (`CXP_LS_MODE.LS_RATE`), with IDLE between packets.
- **Connections.** The IP package builds one connection. Builds with 2 and 4 connections, for cameras on several coax cables, are available on request.

2.3 Packet handling

Table 2-1. What the core does with each packet type on the downlink.

PACKET	WHERE IT GOES	SOFTWARE SEES
Stream data	Tag and size checks, image header and line markers, pixel path, `video_out`	Last stream packet and image header registers, FRAME interrupt, `FRAMES_RECV`
Control acknowledge	Acknowledge FIFO	Code, size, tag and data registers, CNTRL_ACK interrupt
Event	Event FIFO; acknowledged by the core with **Event acknowledge** = By the core	Tag, size and data registers, EVENT interrupt
Heartbeat	Host ID check, time stamp	Device time in two registers, HRTBT interrupt, `HRTBT_RECV`
High-speed trigger	Acknowledged by the core with **Trigger acknowledge** = By the core	`TRIGGER_STATUS`, TRIG interrupt

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

PACKET	WHERE IT GOES	SOFTWARE SEES
Trigger acknowledge		TRIG_ACK interrupt
Test packet	Checked against the test pattern	Good and bad test packet counters

A packet with a bad K code, a CRC error, a size error or the wrong Host ID is counted in its error counter and sets a sticky flag in `CXP_ERRORS_HS`, which raises the HS_ERR interrupt. Bad packets are never passed on as data.

2.4 Video bus

The video output is an AXI4-Stream in the AMD UG934 video convention, with nothing added and nothing left out:

01 Pixel order
Pixel 0, the first in time, sits in the least significant bits. Pixels are packed tight, with no padding between them.

02 Component order
A pixel is its components packed tight, in the UG934 order of its layout.

03 Component width
Every component has `VID_BPC` bits on the bus. A narrower link depth is MSB-aligned with zero LSBs; a wider one loses its LSBs.

04 Padding
`tdata` is padded with zeros at the top to a whole number of bytes; bits a format does not use are zero.

05 Framing
`tuser[0]` marks the first beat of a frame, `tlast` the last beat of every line.

Three parameters size the bus: `VID_PPC` (2 or 4 pixels per beat), `VID_BPC` (8 to 16 bits per component) and `VID_CPP` (1 to 3 components per pixel). The IP GUI derives `VID_CPP` and the `tdata` width from the formats you switch on.

Table 2-2. `tdata` width in bits by components per pixel (`VID_CPP`), pixels per beat (`VID_PPC`) and bits per component (`VID_BPC`). The IP GUI derives it from the format switches. Shaded: the default.

VID_CPP	VID_PPC	BPC 8	BPC 10	BPC 12	BPC 14	BPC 16
1 Mono, Bayer, Raw	2	16	24	24	32	32
	4	32	40	48	56	**64**
2 adds YCbCr 4:2:2 and 4:2:0	2	32	40	48	56	64
	4	64	80	96	112	128
3 adds RGB and YCbCr 4:4:4	2	48	64	72	88	96
	4	96	120	144	168	192

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

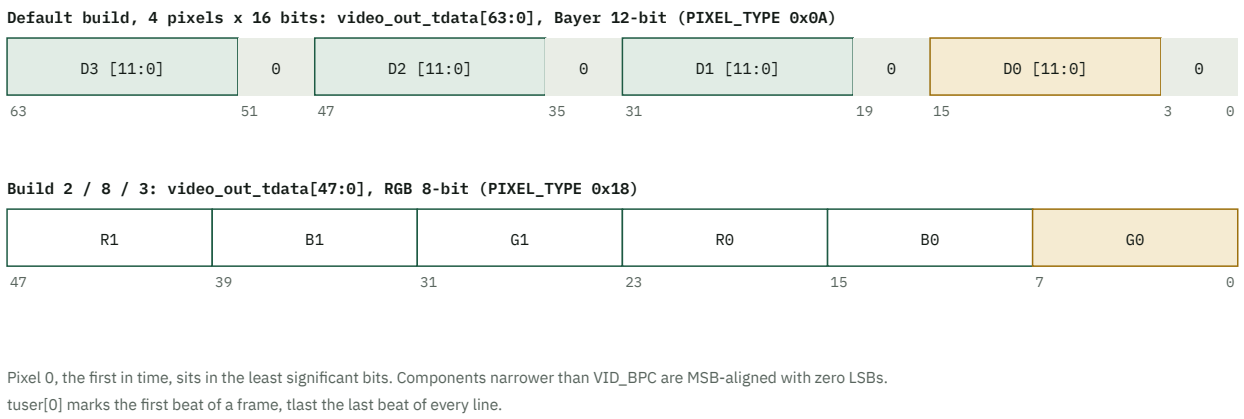


Figure 2-2. Two video beats: the default 64-bit build carrying Bayer 12-bit, and a 2 / 8 / 3 build carrying RGB 8-bit.

AMD video IP uses the same three numbers under other names (Samples per Clock, Maximum Data Width, Number of Video Components). With equal numbers on both sides the buses connect directly. Where an AMD IP has no 14-bit option, build the core with `VID_BPC` = 16 and the 14-bit data arrives MSB-aligned in 16.

2.5 Pixel formats

The camera states its pixel format in the image header; software selects the same format in `PIXEL_TYPE`. The code is {layout, bit depth on the link}:

Table 2-3. `PIXEL_TYPE` codes: bits [7:4] select the layout, bits [3:0] the bit depth on the link (8 = 8-bit to C = 16-bit). 0x00 is accepted as RGB 8-bit, the code of earlier releases.

LAYOUT	8-BIT	10-BIT	12-BIT	14-BIT	16-BIT	COMPONENTS, LSB FIRST	BUILT BY
Mono / Bayer / Raw	0x08	0x09	0x0A	0x0B	0x0C	the sample	VID_EN_MONO
RGB	0x18	0x19	0x1A	0x1B	0x1C	G, B, R	VID_EN_RGB
YCbCr 4:4:4	0x28	0x29	0x2A	0x2B	0x2C	Y, Cb, Cr	VID_EN_YCBCR444
YCbCr 4:2:2	0x38	0x39	0x3A	0x3B	0x3C	Y, C (Cb even pixels, Cr odd)	VID_EN_YCBCR422
YCbCr 4:2:0	0x48	0x49	0x4A	0x4B	0x4C	Y, C (C on even lines only)	VID_EN_YCBCR420

- **Built by switch.** Each layout has a switch in the IP GUI and **Bit depths on the link** picks the depths. Mono / Bayer at every depth is the default. With everything on, one build carries 25 formats. `VIDEO_CAP` reports what was built, and `PIXEL_TYPE.NOT_BUILT` flags a code the bitstream has no path for.
- **Run-time selection.** A write to `PIXEL_TYPE` restarts the stream path with the new format. Write it with the acquisition stopped.
- **Format port.** The same code leaves the core on `pixel_type_out`, so a packer or ISP behind `video_out` follows the one register write without a second register or a GPIO. It changes one AXI4-Lite clock after the write and at no other time.
- **YCbCr 4:2:0.** CoaXPress has no packed 4:2:0 format, so the link carries YCbCr 4:2:2. With a 4:2:0 code the core delivers UG934 4:2:0 (chroma on even lines only); with the 4:2:2 code the same stream comes out as 4:2:2. Any 4:2:2 camera can feed a 4:2:0 consumer such as an encoder.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

2.5.1 Lines and frames

- A line is a multiple of 4 pixels. A YCbCr 4:2:2 line of 4*n* + 2 pixels is accepted at 4 pixels per beat; its last beat has pixels 2 and 3 zero, as UG934 asks.
- Every line starts in a new link word and the core drops the zero padding of the last word of a line.
- A line that breaks the width rule still ends with `tlast`. It is flagged in `PIXEL_TYPE.LINE_ERR`, counted in `PIX_LINE_ERRS` and raises PIX_LINE_ERR.
- Everything before the first start of frame is discarded, so the first thing out is a whole frame. A start of frame inside a line starts a new frame and is flagged the same way.
- Line and frame size are checked against the image header and counted in `FRAME_XSIZE_ERRS` and `FRAME_YSIZE_ERRS`.

2.5.2 Throughput

Table 2-4. Pixel path throughput: share of the link words of one connection the path takes per word clock, and the pixel rate one CXP-12 connection carries.

FORMAT	2 PIXELS PER BEAT	4 PIXELS PER BEAT	MPX/S AT CXP-12
Mono / Bayer 8-bit	50 %	100 %	1220
Mono / Bayer 10-bit	62 %	100 %	976
Mono / Bayer 12-bit	75 %	100 %	813
Mono / Bayer 14-bit	87 %	100 %	697
Mono / Bayer 16-bit	100 %	100 %	610
YCbCr 4:2:2 8 / 10 / 12-bit	100 %	100 %	610 / 488 / 407
RGB or YCbCr 4:4:4 8 / 10 / 12-bit	100 %	100 %	407 / 325 / 271

The video clock must carry the pixel rate: `video_out_clk` ≥ pixels per second / `VID_PPC`. A colour pipeline loses nothing at 2 pixels per beat; Mono and Bayer formats below 16 bits need 4 pixels per beat to use a whole connection.

2.6 Control channel

Software reads and writes the camera's registers, its bootstrap registers and its GenICam description through the control channel. The core builds the packet, sends it on the uplink and collects the acknowledge:

01 Build
Write the command and size to `CXP_CTRL_TX_CMD`, the camera address to `CXP_CTRL_TX_ADDR`, and for a write the data words to `CXP_CTRL_FIFO`.

02 Send
Write `CXP_LS_SEND.CTRL_CMD`. With `CXP_LS_MODE.TAGGED` = 1 the command carries the tag in `CXP_CTRL_TX_TAG` (CXP 2.x); with 0 it is untagged, as used for discovery.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

03 Acknowledge

The CNTRL_ACK interrupt fires when the acknowledge is in. Read the code, size and tag, then the data words from `CXP_CTRL_ACK_FIFO`.

Acknowledges with a CRC, size or tag error are counted and flagged. The supplied driver wraps the sequence in read and write calls.

2.7 Events, triggers and heartbeat

Table 2-5. Asynchronous traffic.

FUNCTION	DIRECTION	BEHAVIOUR
Events	Camera to Host	Each event packet lands in the event FIFO (512 to 2,048 words) with its tag and size, and raises EVENT. Software acknowledges it with `CXP_EVENT_ACK`, or the core does when built with **Event acknowledge** = By the core.
Triggers to the camera	Host to camera	A write to `CXP_LS_SEND.TRIG` sends a trigger on the uplink; the camera's acknowledge raises TRIG_ACK.
Triggers from the camera	Camera to Host	A high-speed trigger raises TRIG and updates `TRIGGER_STATUS`. The core acknowledges it by default (**Trigger acknowledge** = By the core), or software does with `CXP_LS_SEND.TRIG_ACK`.
Heartbeat	Camera to Host	Each heartbeat is checked against the Host ID in `CXP_MASTER_ID`, its 64-bit camera time is kept in two registers, and HRTBT is raised.
Connection test	Both	`CXP_LS_SEND.TEST_START` and `TEST_STOP` run test packets on the uplink; test packets from the camera are checked and counted good or bad.

2.8 Line rate change

CoaXPress starts at a discovery speed and moves to the operating speed once the camera has been configured. In the Host core that is one register write: set the speed code and `CXP_RATE_TRANS.APPLY`. The core then

01 Rewrites the transceiver

DRP writes to the channel and common PLL for the new rate, from tables built into the core for GTH or GTY.

02 Resets it

A PLL and datapath reset on `reset_PLL`, held at least the minimum time.

03 Waits for it

The transceiver must take the reset and report reset done within the timeouts set in the IP GUI; the core retries the reset up to the configured number of times.

04 Reports

RATE_DONE, or RATE_ERR with an error code in `CXP_STATUS[15:14]`. `RATE_CHANGE_CNT` counts completed changes.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

A request is taken in any state, also with the transceiver down, and a request that arrives during a change runs next (newest wins). The timeouts are set in the GUI as times; the GUI converts them with the AXI4-Lite clock frequency.

Table 2-6. Line rate change error codes, `CXP_STATUS[15:14]`. After an error the core is idle again and takes the next request.

CODE	MEANING	WHAT TO CHECK
1	**DRP no answer**	The transceiver did not answer the DRP writes in time. The transceiver is not reset; check the DRP clock and connection.
2	**Reset not acknowledged**	The transceiver wrapper never took the PLL and datapath reset: `reset_PLL` is not connected to it.
3	**Reset done never back**	`reset done` did not return after the retries: the PLL is not locking (reference clock, or the board).

2.9 Interrupts

Fourteen sources feed one interrupt output, `cxp_int`. `ISR` holds a sticky bit per source whether or not it is enabled, `IER` enables sources, `IPR` = ISR and IER shows what drives the output, `GLBL_IER` gates the output, and `IRQ_TEST` sets ISR bits from software to test a handler. The output is a level; after every write to `ISR` it drops for four clocks and returns if anything is still pending, so an edge-triggered input sees every event too. The bit list is in ISR.

2.10 Buffering and overflow

Table 2-7. Buffers, set in the IP GUI.

BUFFER	GUI FIELD	SIZES	HOLDS
Control FIFOs	Control FIFOs (words)	`1024, 2048, 4096`	Command data out and acknowledge data in
Event FIFO	Event FIFO (words)	`512, 1024, 2048`	Event packets waiting for software
Stream FIFO	Stream FIFO (words)	`2048 to 16384`	Link words between the parser and the pixel path
Video FIFO	Video output FIFO (beats)	`512 to 4096`	Beats waiting for `video_out_tready`, crossing to the video clock

A camera cannot be paused. When the video sink holds `tready` low long enough for the video and stream FIFOs to fill, the core drops stream words rather than stall the link, counts them in `VIDEO_OVF_ERRS`, raises VIDEO_OVF and shows the FIFO state in `CXP_STATUS`. Size the video FIFO for the longest stall of your sink; it costs block RAM only, about one BRAM36 per 512 beats of a 64-bit bus.

2.11 Clocks and reset

Table 2-8. Clock domains.

CLOCK	SOURCE	RUNS
`rx_outclk2`	Word clock from the transceiver wrapper: line rate / 40, 312.5 MHz at CXP-12; changes with the speed	The receive path, parser and pixel path

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

CLOCK	SOURCE	RUNS
aclk	Free-running clock, 50 to 300 MHz, set in the GUI so the line rate change timeouts are right	Register file, interrupt controller, line rate change
video_out_clk	The clock of the block that takes the video, any frequency that carries the pixel rate	The read side of the video FIFO and `video_out`
drp_clk	Output of the core to the transceiver wrapper	DRP accesses for the line rate change

- Clock `aclk` from a free-running clock. The registers stay readable while the link is down, and software reads ID and VERSION at boot before any camera is plugged in.
- Every crossing uses AMD XPM macros and constrains itself. Enable the XPM libraries in the project; do not add clock groups or false paths between these clocks.
- `reset_PLL` must reach the PLL and datapath reset of the transceiver wrapper, as in the example designs. Without it a line rate change ends with error code 2 or 3.
- `RST_CXP` pulses resets for the whole core, the high-speed paths and the uplink, so software can recover any part without a reconfiguration.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 03

Interfaces and Timing

IP parameters by GUI page, every interface of the core, the video output timing and the integration checklist.

3.1 IP customization parameters

Every setting in the IP GUI is a drop-down list; fields the GUI works out are shown read-only. Software reads the build back from `HWCFG` and `VIDEO_CAP`, so one driver serves every build. Defaults are in bold.

3.1.1 Link

Table 3-1. Link page.

GUI FIELD	PARAMETER	VALUES	DESCRIPTION
Transceiver	TRANSCEIVER_TYPE	**GTY (GTYE4)**, GTH (GTHE4)	Selects the DRP rate tables for the line rate change.
Connections	NUM_LANES	**1**	Coax connections. 2 and 4 on request.
AXI4-Lite clock (aclk)	ACLK_FREQ_MHZ	50, **100**, 125, 150, 200, 250, 300 MHz	Frequency of `aclk`; converts the line rate change timeouts to clock cycles.
Trigger acknowledge	TRIG_AUTO_ACK	**By the core**, By software	Who acknowledges a high-speed trigger from the camera.
Event acknowledge	EVENT_AUTO_ACK	By the core, **By software**	Who acknowledges an event packet.

3.1.2 Video

Table 3-2. Video page.

GUI FIELD	PARAMETER	VALUES	DESCRIPTION
Mono / Bayer	VID_EN_MONO	**Built**, Not built	Mono, Bayer and Raw layouts, 1 component.
RGB	VID_EN_RGB	Built, **Not built**	RGB, 3 components.
YCbCr 4:4:4	VID_EN_YCBCR444	Built, **Not built**	3 components.
YCbCr 4:2:2	VID_EN_YCBCR422	Built, **Not built**	2 components.
YCbCr 4:2:0	VID_EN_YCBCR420	Built, **Not built**	4:2:0 on the bus, 4:2:2 on the link.
Bit depths on the link	VID_LINK_WIDTHS	**8, 10, 12, 14 and 16-bit**, or any subset	The larger saving: each depth is a gearbox of its own.
Pixels per beat	VID_PPC	2, **4**	Pixels per `video_out` beat.
Bits per component	VID_BPC	8, 10, 12, 14, **16**	Component width on the bus.
Components per pixel	VID_CPP	read-only, **1**	3 with RGB or YCbCr 4:4:4, 2 with YCbCr 4:2:2 or 4:2:0, else 1.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

GUI FIELD	PARAMETER	VALUES	DESCRIPTION
TDATA width (bit)	MAX_TDATA_WIDTH	read-only, **64**	`VID_PPC` x `VID_CPP` x `VID_BPC`, rounded up to whole bytes.
Pixel format after reset	PIXEL_TYPE_DEFAULT	25 codes, **Mono / Bayer 8-bit (0x08)**	Reset value of `PIXEL_TYPE` and `pixel_type_out`.

3.1.3 Buffers

Table 3-3. Buffers page.

GUI FIELD	PARAMETER	VALUES
Control FIFOs (words)	CMD_PCKT_MAX	**1024**, 2048, 4096
Event FIFO (words)	EVENT_PCKT_MAX_SIZE	**512**, 1024, 2048
Stream FIFO (words)	STREAM_FIFO_DEPTH	**2048**, 4096, 8192, 16384
Video output FIFO (beats)	AXI4S_DEPTH	**512**, 1024, 2048, 4096

3.1.4 Advanced

Table 3-4. Advanced page.

GUI FIELD	PARAMETER	VALUES
Synchronizer flops	SYNC_STAGE	2, 3, **4**, 5, 6
IDLE words for lock	IDLE_LOCK_CNTR	**64**, 128, 256, 512, 1024
Words without IDLE for an error	IDLE_ERR_NUM	50, **100**, 200, 500, 1000
Extra reset attempts	RECONFIG_RETRIES	0, 1, **2**, 3
DRP timeout	RECONFIG_DRP_TIMEOUT_US	**1 ms**, 2, 5, 10 ms
Reset acknowledge timeout	RECONFIG_RST_ACK_TIMEOUT_US	**100 µs**, 1, 10, 100 ms
Reset done timeout	RECONFIG_DONE_TIMEOUT_US	**20 ms**, 50, 100, 200 ms

From a block design script, for a Mono / Bayer and RGB build at 2 pixels of 8 bits on a GTH:

```
set_property -dict [list \
    CONFIG.TRANSCEIVER_TYPE {GTHE4} \
    CONFIG.ACLK_FREQ_MHZ    {100} \
    CONFIG.VID_PPC          {2} \
    CONFIG.VID_BPC          {8} \
    CONFIG.VID_EN_RGB       {1} \
    CONFIG.VID_LINK_WIDTHS  {1} \
    CONFIG.PIXEL_TYPE_DEFAULT {24} \
] [get_bd_cells cxp_host_0]
```

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

Leave `VID_CPP` and `MAX_TDATA_WIDTH` out of scripts: the GUI derives them from the switches.

3.2 Interface overview

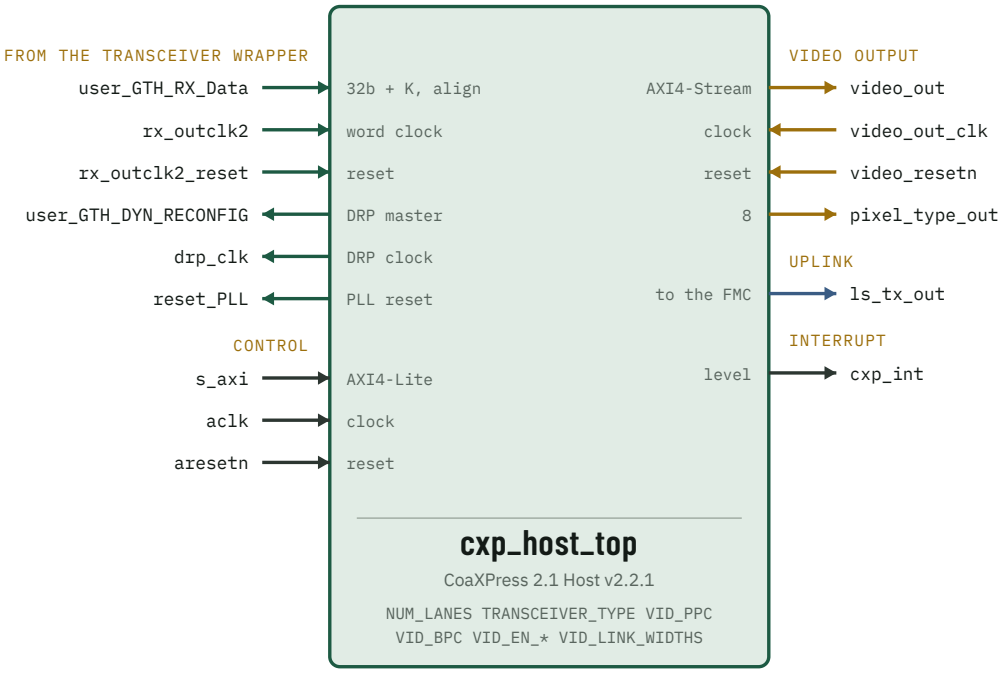


Figure 3-1. IP symbol. Green interfaces connect to the supplied transceiver wrapper, gold ones are the video output, blue is the uplink to the FMC, dark ones are control.

3.3 Interface descriptions

3.3.1 Transceiver wrapper

Table 3-5. Connections to the supplied transceiver wrapper. Connect them as in the example designs.

INTERFACE	DIR	TYPE	DESCRIPTION
`user_GTH_RX_Data`	in/out	bus	Received 32-bit words and K flags of the connection, and the word alignment control
`rx_outclk2`	in	clock	Word clock, line rate / 40
`rx_outclk2_reset`	in	reset	Reset of the word clock domain from the wrapper
`user_GTH_DYN_RECONFIG`	out/in	DRP	DRP master used for the line rate change
`drp_clk`	out	clock	DRP clock to the wrapper
`reset_PLL`	out	reset	PLL and datapath reset request. Must reach the wrapper's PLL and datapath reset

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

3.3.2 AXI4-Lite control and interrupt

Table 3-6. Register interface and interrupt.

INTERFACE	DIR	WIDTH	DESCRIPTION
s_axi	slave	addr 12, data 32	AXI4-Lite. Write address and write data are accepted in either order. A refused access (unmapped offset, empty FIFO read, full FIFO write, a connection count the build does not have) answers SLVERR; a read the register block does not answer within 255 clocks answers SLVERR instead of hanging the bus
aclk	in	1	Register clock, free-running, independent of every other clock
aresetn	in	1	Active-low reset on `aclk`
cxp_int	out	1	Interrupt, active high level; drops for 4 clocks after each `ISR` write and returns while sources are pending

3.3.3 Video output

Table 3-7. AXI4-Stream video master video_out and the format port.

PORT	DIR	WIDTH	DESCRIPTION
video_out_clk	in	1	Video clock, any frequency ≥ pixel rate / `VID_PPC`, no relation to the word clock
video_resetn	in	1	Active-low reset on `video_out_clk`
video_out_tdata	out	MAX_TDATA_WIDTH	UG934 beat: `VID_PPC` pixels, pixel 0 in the LSBs
video_out_tvalid	out	1	Held with the payload until `tready`
video_out_tready	in	1	May change on any clock
video_out_tuser	out	1	Start of frame: first beat of the first line
video_out_tlast	out	1	End of line: last beat of every line
pixel_type_out	out	8	`PIXEL_TYPE[7:0]` on `aclk`, a register output; changes one clock after a write. 0x00 comes out as 0x18. Synchronize it before use in another clock domain, or leave it open

3.3.4 Uplink

Table 3-8. Low-speed uplink.

PORT	DIR	WIDTH	DESCRIPTION
ls_tx_out	out	1	Uplink bit stream to the CoaXPress driver on the FMC, 20.83 or 41.67 Mb/s

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

3.4 Video output timing

Standard AXI4-Stream rules: `tvalid` and the payload hold until the handshake, and `tready` may do anything. The first capture shows a whole frame of three short lines; the second shows the beat level with a sink stall.

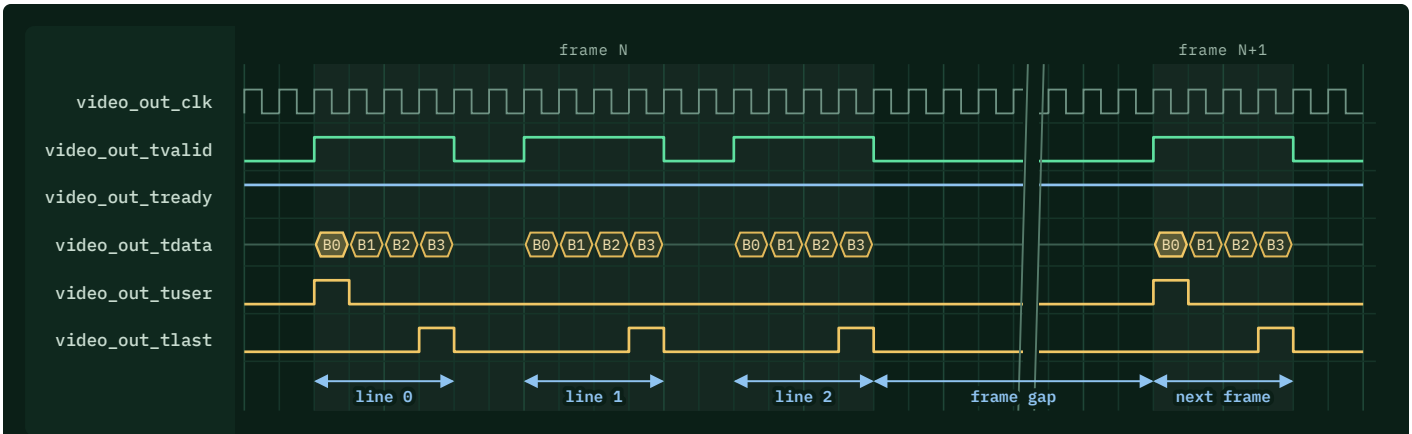


Figure 3-2. `video_out` over one frame of three short lines (4 beats each), then the first beats of the next frame. Every port of the interface is shown.

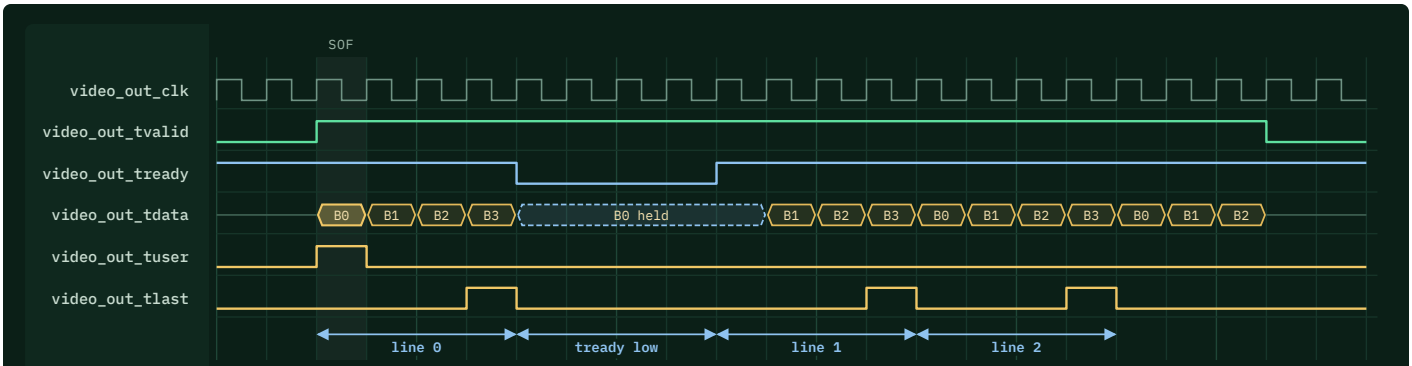


Figure 3-3. `video_out` at the beat level: start of frame on the first beat, end of line on every fourth beat, and a sink stall that holds the next beat on the bus until `tready` returns.

Between lines and frames `tvalid` is low. Lines come out at the pace the camera sends them; the video FIFO absorbs the difference between the link and the video clock within a line.

3.5 Integration checklist

- XPM libraries enabled in the Vivado project.
- `reset_PLL` connected to the transceiver wrapper's PLL and datapath reset.
- `cxp_int` connected as a level, active high, or as an edge.
- A 4 KB address range for `s_axi` in the Vivado address editor.
- **AXI4-Lite clock** in the GUI set to the real `aclk` frequency.
- Software writes `PIXEL_TYPE` to the camera's pixel format, or `PIXEL_TYPE_DEFAULT` is what the camera sends.
- `pixel_type_out` wired to the packer or ISP behind `video_out`, if it has a format input.
- `video_out_clk` fast enough for the pixel rate at `VID_PPC` pixels per beat.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 04

Register Map

Eighty-three 32-bit registers on AXI4-Lite in a 4 KB window: identification and interrupts, video, link control, the control channel, events, the image header, and the error and statistics counters.

4.1 Register interface

- AXI4-Lite slave, 32-bit data, 12-bit byte address: a 4 KB window. Offsets are byte offsets from the base address assigned in the Vivado address editor.
- Access types: RO read-only, RW read/write, WO write-only, WP write pulses an action and reads 0, W1C write 1 to clear, W1S write 1 to set, RC counter that takes any written value (write 0 to clear; reading does not clear).
- The core answers SLVERR for an access it refuses: an unmapped offset, a read of an empty FIFO, a write to a full FIFO, a connection count the build does not have. On a Zynq that is a data abort, so software never probes blindly; the supplied driver never does it.
- The first four words (ID, VERSION, HWCFG, SCRATCH) follow the same layout in every ApotheoTech core, so one probe routine identifies any of them.

4.2 Register summary

Table 4-1. Register summary. Offsets are byte offsets from the core base address; the core decodes a 4 KB window. Offsets not listed are reserved.

OFFSET	NAME	ACCESS	FUNCTION
IDENTIFICATION AND INTERRUPTS			
0x000	ID	RO	Core identification word
0x004	VERSION	RO	Core release, major.minor.patch
0x008	HWCFG	RO	Build parameters of this instance
0x00C	SCRATCH	RW	Software scratch word
0x010	RST_CXP	WP	Reset pulses
0x014	GLBL_IER	RW	Global interrupt enable
0x018	ISR	W1C	Interrupt status, sticky
0x01C	IER	RW	Interrupt enable
0x020	IPR	RO	Interrupt pending = ISR and IER
0x024	IRQ_TEST	W1S	Set ISR bits from software
VIDEO AND CONNECTIONS			
0x028	PIXEL_TYPE	RW	Pixel format {layout, link bit depth}
0x02C	STREAM_LANES	RW	Connections that carry stream packets

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	FUNCTION
0x030	VIDEO_CAP	RO	Video bus of this build
0x034	LANE_STATUS	RO	Lock per connection
LINK STATUS AND CONTROL			
0x050	CXP_STATUS	RO	Transceiver, lock, FIFO and line rate status
0x054	CXP_ERRORS_HS	W1C	High-speed error flags, sticky
0x058	CXP_ERRORS_LS	W1C	Low-speed error flags, sticky
0x05C	CXP_RATE_TRANS	RW	Line rate change request
0x064	STREAM_PCKT_MAX	RW	Largest stream packet accepted
0x070	CXP_LS_MODE	RW	Uplink mode
0x074	CXP_LS_SEND	WP	Send on the uplink
CONTROL CHANNEL			
0x078	CXP_CTRL_TX_CMD	RW	Control command and size
0x07C	CXP_CTRL_TX_ADDR	RW	Address in the Device
0x080	CXP_CTRL_TX_TAG	RO	Tag the next tagged command will carry
0x084	CXP_CTRL_FIFO	WO	Command data FIFO
0x098	CXP_CTRL_ACK_CODE	RO	Acknowledge code
0x09C	CXP_CTRL_ACK_SIZE	RO	Acknowledge size in bytes
0x0A0	CXP_CTRL_ACK_TAG	RO	Acknowledge tag
0x0A4	CXP_CTRL_ACK_FIFO	RO	Acknowledge data FIFO
0x0A8	CXP_ACK_FIFO_ENTRY	RO	Words in the acknowledge FIFO
0x0BC	CXP_MASTER_ID	RW	Host connection ID
EVENTS, TRIGGERS AND HEARTBEAT			
0x08C	CXP_EVENT_ACK	RW	Event acknowledge
0x094	TRIGGER_STATUS	RO	Last high-speed trigger
0x0AC	CXP_EVENT_TAG	RO	Tag of the last event packet
0x0B0	CXP_EVENT_SIZE	RO	Size of the last event packet
0x0B4	CXP_EVENT_FIFO	RO	Event data FIFO
0x0B8	CXP_EVENT_FIFO_ENTRY	RO	Words in the event FIFO
0x0C0	CXP_HRTBT_TIME_REG0	RO	Device time [63:32]
0x0C4	CXP_HRTBT_TIME_REG1	RO	Device time [31:0]

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	FUNCTION
STREAM AND IMAGE HEADER			
0x0C8	CXP_STRM_ID_TAG_SIZE	RO	Last stream packet
0x0CC	CXP_FRM_ID_TAG_FLAG	RO	Last image header: IDs and flags
0x0D0	CXP_XSIZE	RO	Last image header: Xsize
0x0D4	CXP_XOFFS	RO	Last image header: Xoffs
0x0D8	CXP_YSIZE	RO	Last image header: Ysize
0x0DC	CXP_YOFFS	RO	Last image header: Yoffs
0x0E0	CXP_FRM_DSIZE	RO	Last image header: DsizeL, words per line
0x0E4	CXP_PIXELF_TAPG	RO	Last image header: PixelF and TapG
CONNECTION TEST			
0x090	CXP_TEST_PCKTS_SENT	RC	Test packets sent on the uplink
0x0E8	CXP_TEST_PCKTS_RECV	RO	Good test packets received on the downlink, connection 0
0x0EC	CXP_TEST_RECV_ERRS	RO	Bad test packets received on the downlink, connection 0
ERROR COUNTERS			
0x0F0	STREAM_K_CODE_ERRS	RC	Stream packets with a bad K code
0x0F4	STREAM_CRC_ERRS	RC	Stream packets with a CRC error
0x0F8	STREAM_DSIZEP_ERRS	RC	Stream packets whose size does not match DsizeP
0x0FC	STREAM_PCKT_MAX_ERRS	RC	Stream packets larger than STREAM_PCKT_MAX
0x100	FRAME_XSIZE_ERRS	RC	Line length errors against the image header (Xsize)
0x104	FRAME_YSIZE_ERRS	RC	Frame height errors against the image header (Ysize)
0x108	PIXEL_FMT_ERRS	RC	Pixel format errors in the image header
0x10C	CNTRL_K_CODE_ERRS	RC	Control acknowledges with a bad K code
0x110	CNTRL_CRC_ERRS	RC	Control acknowledges with a CRC error
0x114	CNTRL_TAG_N_EXP_ERRS	RC	Control acknowledges with a tag when none was expected
0x118	CNTRL_TAG_EXP_ERRS	RC	Control acknowledges without the expected tag
0x11C	CNTRL_SIZE_ERRS	RC	Control acknowledges with a size error
0x120	CNTRL_TAG_ERRS	RC	Control acknowledges with the wrong tag
0x124	EVENT_MSTR_ID_ERRS	RC	Event packets for another Host ID
0x128	EVENT_MALF_ERRS	RC	Malformed event packets
0x12C	EVENT_K_CODE_ERRS	RC	Event packets with a bad K code

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	FUNCTION
0x130	EVENT_CRC_ERRS	RC	Event packets with a CRC error
0x134	HRTBT_MSTR_ID_ERRS	RC	Heartbeats for another Host ID
0x138	HRTBT_MALF_ERRS	RC	Malformed heartbeats
0x13C	HRTBT_K_CODE_ERRS	RC	Heartbeats with a bad K code
0x140	LS_CMD_FIFO_EMPTY_ERRS	RC	Uplink command FIFO empty errors
0x144	LS_CMD_SIZE_ERRS	RC	Uplink command size errors
STATISTICS			
0x148	STREAM_PCKTS_RECV_TOT	RC	Stream packets seen
0x14C	STREAM_PCKTS_RECV_SUCC	RC	Stream packets that ended cleanly
0x150	STREAM_XSIZE_CNTR_ERR	RO	Words counted in the line that raised FRAME_XSIZE
0x154	STREAM_YSIZE_CNTR_ERR	RO	Lines counted in the frame that raised FRAME_YSIZE
0x158	VIDEO_OVF_ERRS	RC	Stream words dropped because the video path was full
0x15C	PIX_LINE_ERRS	RC	Lines that broke the width rule of the pixel format
0x160	FRAMES_RECV	RC	Image headers received
0x164	HRTBT_RECV	RC	Heartbeat packets received
0x168	LOSS_LOCK_CNT	RC	Loss of lock events, all connections
0x16C	RATE_CHANGE_CNT	RC	Completed line rate changes
0x170	STREAM_TAG_ERRS	RC	Stream packet tag jumps (lost packets)

Read-only Read/write Write pulse, action Write 1 to clear Reserved

4.3 Identification and interrupts

Read ID and VERSION before any write: they confirm the base address and the release. HWCFG and VIDEO_CAP tell software how the core was built.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

0x000 ID RO

reset 0xA71C0A01

Fixed identification word. Software reads it first: it proves that the base address points at this core.



BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:20]	VENDOR	RO	0xA71	Vendor code: 0xA71 = ApotheoTech.
[19:8]	CORE	RO	0xC0A	Core code: 0xC0A = CoaXPress.
[7:0]	FUNCTION	RO	0x01	Function: 0x01 = Host.

0x004 VERSION RO

reset 0x02020001

Release of the core in the bitstream. A new major number means another register map; a new minor number is a compatible addition; a patch has no software-visible change.



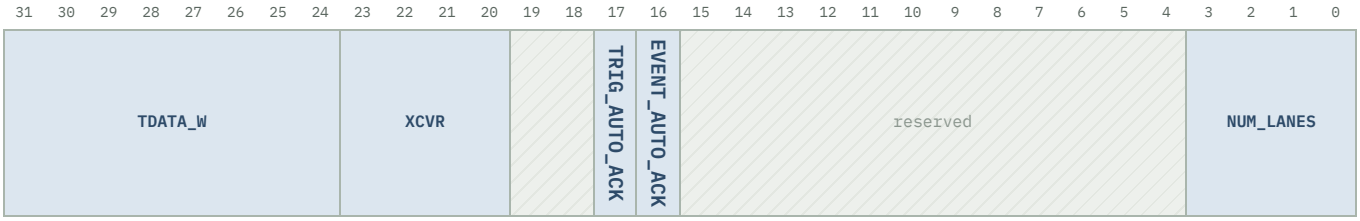
BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:24]	MAJOR	RO	0x02	Major version: register map generation.
[23:16]	MINOR	RO	0x02	Minor version.
[15:0]	PATCH	RO	0x0001	Patch level.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

0x008 HWCFG RO

reset build

The generics the core was built with, so one driver serves every build.



BITS	FIELD	ACCESS	DESCRIPTION
[31:24]	TDATA_W	RO	`video_out` tdata width in bits.
[23:20]	XCVR	RO	Transceiver: 0 GTH (GTHE4), 1 GTY (GTYE4).
[19:18]	reserved		Reserved.
[17]	TRIG_AUTO_ACK	RO	1 = the core acknowledges high-speed triggers itself.
[16]	EVENT_AUTO_ACK	RO	1 = the core acknowledges event packets itself.
[15:4]	reserved		Reserved.
[3:0]	NUM_LANES	RO	Connections built.

0x00C SCRATCH RW

reset 0x00000000

Reads back what was written, byte strobes honoured. No effect on the core.



BITS	FIELD	ACCESS	RESET	DESCRIPTION
[31:0]	SCRATCH	RW	0	Any value.

0x014 GLBL_IER RW

reset 0x00000000

Bit 0 enables the interrupt output `cxp_int`.



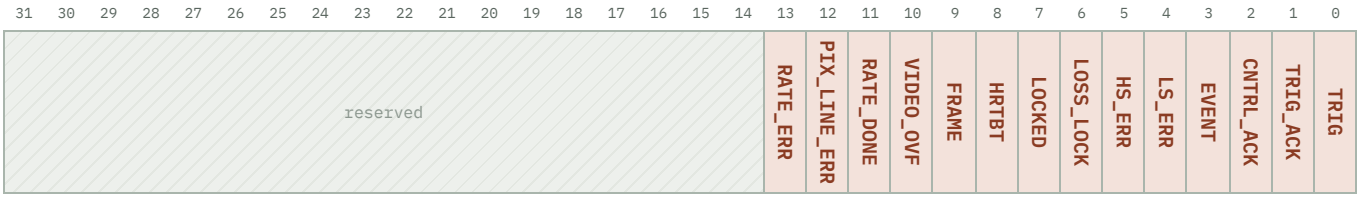
BITS	FIELD	ACCESS	DESCRIPTION
[31:1]	reserved		Reserved.
[0]	GIE	RW	1 = `cxp_int` may assert.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

0x018 ISR W1C

reset 0x00000000

One sticky bit per source, set by the core whether or not the source is enabled. Write 1 to clear. A source that fires in the clock it is cleared is kept.



BITS	FIELD	ACCESS	DESCRIPTION
[31:14]	reserved		Reserved.
[13]	RATE_ERR	W1C	Line rate change failed, code in CXP_STATUS[15:14].
[12]	PIX_LINE_ERR	W1C	A line broke the width rule of the pixel format.
[11]	RATE_DONE	W1C	Line rate change finished, receiver back.
[10]	VIDEO_OVF	W1C	Stream words dropped: the video path was full.
[9]	FRAME	W1C	Image header received.
[8]	HRTBT	W1C	Heartbeat received.
[7]	LOCKED	W1C	All connections in use are locked.
[6]	LOSS_LOCK	W1C	A connection lost lock.
[5]	HS_ERR	W1C	A CXP_ERRORS_HS flag was set.
[4]	LS_ERR	W1C	A CXP_ERRORS_LS flag was set.
[3]	EVENT	W1C	Event packet received.
[2]	CNTRL_ACK	W1C	Control acknowledge received.
[1]	TRIG_ACK	W1C	Trigger acknowledge received.
[0]	TRIG	W1C	High-speed trigger received from the Device.

Table 4-2. Reset and interrupt registers. IER, IPR and IRQ_TEST use the ISR bit positions.

OFFSET	NAME	ACCESS	MEANING
0x010	RST_CXP	WP	Writing a 1 pulses the matching reset: bit 31 resets the whole core, bits [20:16] the high-speed receive paths, bits [15:14] module resets, bits [1:0] the low-speed uplink. Reads 0. The supplied driver names each bit.
0x01C	IER	RW	One enable bit per ISR bit, same positions.
0x020	IPR	RO	The sources that drive the interrupt output now.
0x024	IRQ_TEST	W1S	Write 1 to set the matching ISR bit, to test the interrupt handler without the link.

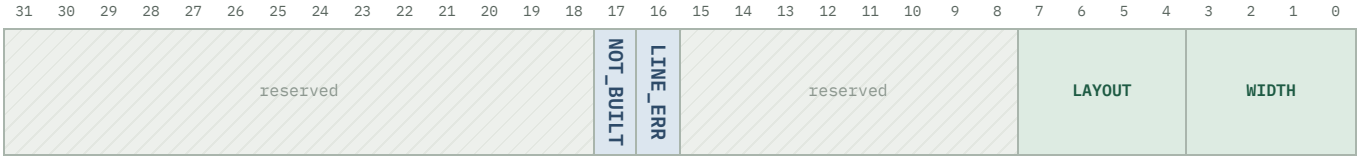
© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

4.4 Video and connections

0x028 PIXEL_TYPE RW

reset generic

Pixel format of the stream: the layout and the bit depth on the link. A write restarts the stream path, so write it with the acquisition stopped. The value also leaves the core on `pixel_type_out`. Resets to `PIXEL_TYPE_DEFAULT`.



BITS	FIELD	ACCESS	DESCRIPTION
[31:18]	reserved		Reserved.
[17]	NOT_BUILT	RO	1 = the code has no path in this bitstream (layout or bit depth not built, or not a code). No video moves until a code that is built is written.
[16]	LINE_ERR	RO	1 = a line broke the width rule of the format, or a frame started inside a line. Sticky until the stream path restarts.
[15:8]	reserved		Reserved.
[7:4]	LAYOUT	RW	0 Mono / Bayer, 1 RGB, 2 YCbCr 4:4:4, 3 YCbCr 4:2:2, 4 YCbCr 4:2:0.
[3:0]	WIDTH	RW	Bit depth on the link: 8 = 8-bit, 9 = 10-bit, A = 12-bit, B = 14-bit, C = 16-bit.

0x030 VIDEO_CAP RO

reset build

What the bitstream was built with, so software can offer only the formats that exist. The default build (4 pixels per beat, 16-bit, Mono / Bayer, every bit depth) reads 0x1F011014.



BITS	FIELD	ACCESS	DESCRIPTION
[31:29]	reserved		Reserved.
[28:24]	WIDTHS	RO	Link bit depths built, bit 24 + (WIDTH - 8): 8, 10, 12, 14, 16-bit.
[23:21]	reserved		Reserved.
[20:16]	LAYOUTS	RO	Layouts built, bit 16 + LAYOUT: Mono / Bayer, RGB, YCbCr 4:4:4, 4:2:2, 4:2:0.
[15:13]	reserved		Reserved.
[12:8]	BPC	RO	VID_BPC, bits per component on the bus.
[7:4]	CPP	RO	VID_CPP, components per pixel the bus has room for.
[3:0]	PPC	RO	VID_PPC, pixels per beat.

Table 4-3. Connection registers.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

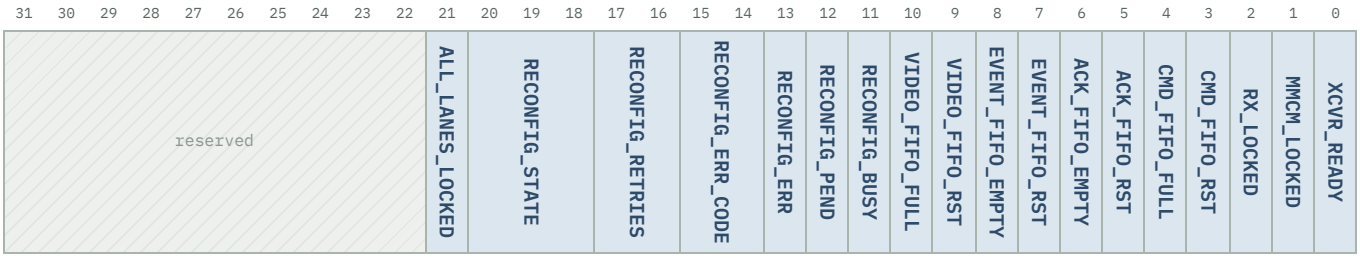
OFFSET	NAME	ACCESS	MEANING
0x02C	STREAM_LANES	RW	Bits [2:0]: 1 to NUM_LANES. Write it with ConnectionConfig and after a ConnectionReset. A value the build does not have is refused with SLVERR.
0x034	LANE_STATUS	RO	Bits [3:0]: connection locked. Bits [11:8]: loss of lock seen since the last read (cleared on read).

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

4.5 Link status and control

0x050 CXP_STATUS RO

Live status of the receiver. Bits [20:11] describe the last line rate request and are laid out the same in the Host and the Device core.

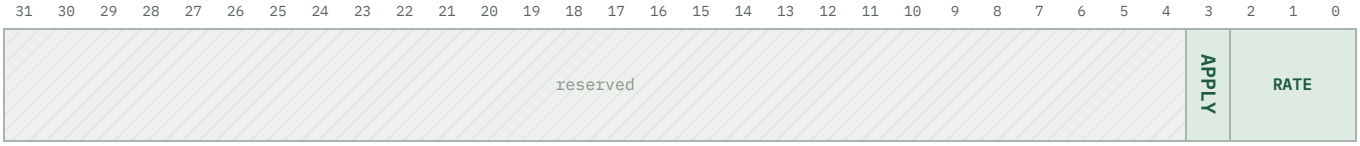


BITS	FIELD	ACCESS	DESCRIPTION
[31:22]	reserved		Reserved.
[21]	ALL_LANES_LOCKED	RO	Every connection in STREAM_LANES is locked.
[20:18]	RECONFIG_STATE	RO	Line rate change state: 0 idle, 1 DRP writes, 2 reset held, 3 waiting for the reset to be taken, 4 waiting for reset done.
[17:16]	RECONFIG_RETRIES	RO	Extra PLL resets the last request needed.
[15:14]	RECONFIG_ERR_CODE	RO	Error of the last request: 1 DRP no answer, 2 reset not acknowledged, 3 reset done never back.
[13]	RECONFIG_ERR	RO	The last request failed.
[12]	RECONFIG_PEND	RO	A request is latched and not yet launched.
[11]	RECONFIG_BUSY	RO	A line rate change is running.
[10]	VIDEO_FIFO_FULL	RO	Video FIFO full.
[9]	VIDEO_FIFO_RST	RO	Video FIFO in reset.
[8]	EVENT_FIFO_EMPTY	RO	Event FIFO empty.
[7]	EVENT_FIFO_RST	RO	Event FIFO in reset.
[6]	ACK_FIFO_EMPTY	RO	Control acknowledge FIFO empty.
[5]	ACK_FIFO_RST	RO	Control acknowledge FIFO in reset.
[4]	CMD_FIFO_FULL	RO	Control command FIFO full.
[3]	CMD_FIFO_RST	RO	Control command FIFO in reset.
[2]	RX_LOCKED	RO	Connection 0 word aligned and locked.
[1]	MMCM_LOCKED	RO	Low-speed clock MMCM locked.
[0]	XCVR_READY	RO	Transceiver reset done.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

0x05C CXP_RATE_TRANS RW

Writing bit 3 = 1 starts a line rate change to the speed in bits [2:0]: the core rewrites the transceiver PLL and dividers over DRP, resets the PLL and datapath, and waits for the transceiver to come back. A request that arrives while one runs is kept (newest wins) and runs next. Progress and errors are in `CXP_STATUS[20:11]`; the RATE_DONE and RATE_ERR interrupts report the end.



BITS	FIELD	ACCESS	DESCRIPTION
[31:4]	reserved		Reserved.
[3]	APPLY	RW	1 = start the rate change.
[2:0]	RATE	RW	Line rate code, CXP-1 to CXP-12. The supplied driver holds the code table.

0x070 CXP_LS_MODE RW

Bit 0: CXP 2.x tagged control commands. Bit 1: uplink rate, 0 = 20.83 Mb/s, 1 = 41.67 Mb/s (CXP-10 and CXP-12).



BITS	FIELD	ACCESS	DESCRIPTION
[31:2]	reserved		Reserved.
[1]	LS_RATE	RW	0 = 20.83 Mb/s, 1 = 41.67 Mb/s.
[0]	TAGGED	RW	1 = tagged control commands (CXP 2.x).

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

0x074 CXP_LS_SEND WP

Writing a 1 sends the matching packet on the uplink: a trigger, a trigger acknowledge, the control command built in the control channel registers, or the connection test start and stop. Reads 0.



BITS	FIELD	ACCESS	DESCRIPTION
[31:8]	reserved		Reserved.
[7]	TEST_START	WP	Start sending test packets.
[6]	TEST_STOP	WP	Stop sending test packets.
[5]	CTRL_CMD	WP	Send the control command.
[4]	TRIG_ACK	WP	Send a trigger acknowledge.
[3:0]	TRIG	WP	Send a trigger.

Table 4-4. Error flags and packet size.

OFFSET	NAME	ACCESS	MEANING
0x054	CXP_ERRORS_HS	W1C	One sticky flag per high-speed error counter (0x0F0 to 0x13C). Write 1 to clear. Any flag raises the HS_ERR interrupt.
0x058	CXP_ERRORS_LS	W1C	One sticky flag per uplink error counter (0x140, 0x144). Write 1 to clear. Any flag raises the LS_ERR interrupt.
0x064	STREAM_PCKT_MAX	RW	Stream packets larger than this are counted in STREAM_PCKT_MAX_ERRS. Set it to the StreamPacketSizeMax negotiated with the Device.

4.6 Control channel

The command is built in these registers and sent with `CXP_LS_SEND.CTRL_CMD`; the acknowledge is read back from the same block. See Control channel.

Table 4-5. Control channel registers.

OFFSET	NAME	ACCESS	MEANING
0x078	CXP_CTRL_TX_CMD	RW	Bits [31:24]: command (read or write). Bits [23:0]: size in bytes.
0x07C	CXP_CTRL_TX_ADDR	RW	Address in the Device.
0x080	CXP_CTRL_TX_TAG	RO	Tag the next tagged command will carry.
0x084	CXP_CTRL_FIFO	WO	Write data of the command, one word per write. A write to a full FIFO is refused with SLVERR.
0x098	CXP_CTRL_ACK_CODE	RO	Bits [7:0]: acknowledge code of the last control acknowledge.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	MEANING
0x09C	CXP_CTRL_ACK_SIZE	RO	Acknowledge size in bytes.
0x0A0	CXP_CTRL_ACK_TAG	RO	Bits [7:0]: tag of the last acknowledge.
0x0A4	CXP_CTRL_ACK_FIFO	RO	Read data of the acknowledge, one word per read. A read of an empty FIFO is refused with SLVERR.
0x0A8	CXP_ACK_FIFO_ENTRY	RO	Words in the acknowledge FIFO.
0x0BC	CXP_MASTER_ID	RW	The ID written to the Device's MasterHostConnectionID at discovery. Event packets and heartbeats for another ID are counted as errors.

4.7 Events, triggers and heartbeat

Table 4-6. Event, trigger and heartbeat registers.

OFFSET	NAME	ACCESS	MEANING
0x08C	CXP_EVENT_ACK	RW	Bits [7:0]: tag. The write sends the event acknowledge (when the core does not acknowledge events itself).
0x094	TRIGGER_STATUS	RO	Bits [15:8]: trigger number. Bits [7:0]: delay of the last high-speed trigger.
0x0AC	CXP_EVENT_TAG	RO	Bits [7:0].
0x0B0	CXP_EVENT_SIZE	RO	Bits [15:0], in words.
0x0B4	CXP_EVENT_FIFO	RO	One word per read. A read of an empty FIFO is refused with SLVERR.
0x0B8	CXP_EVENT_FIFO_ENTRY	RO	Words in the event FIFO.
0x0C0	CXP_HRTBT_TIME_REG0	RO	From the last heartbeat.
0x0C4	CXP_HRTBT_TIME_REG1	RO	From the last heartbeat.

4.8 Stream and image header

The last stream packet and the last rectangular image header as received, for software that checks the camera's geometry and format before it starts its own pipeline.

Table 4-7. Last stream packet and image header, as received.

OFFSET	NAME	ACCESS	MEANING
0x0C8	CXP_STRM_ID_TAG_SIZE	RO	Bits [31:24]: stream ID. Bits [23:16]: packet tag. Bits [15:0]: DsizeP.
0x0CC	CXP_FRM_ID_TAG_FLAG	RO	Bits [31:24]: stream ID. Bits [23:8]: source tag. Bits [7:0]: flags.
0x0D0	CXP_XSIZE	RO	Last image header: Xsize.
0x0D4	CXP_XOFFS	RO	Last image header: Xoffs.
0x0D8	CXP_YSIZE	RO	Last image header: Ysize.
0x0DC	CXP_YOFFS	RO	Last image header: Yoffs.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	MEANING
0x0E0	CXP_FRM_DSIZE	RO	Last image header: DsizeL, words per line.
0x0E4	CXP_PIXELF_TAPG	RO	Bits [31:16]: PixelF. Bits [15:0]: TapG.

4.9 Connection test

Table 4-8. Connection test counters.

OFFSET	NAME	ACCESS	MEANING
0x090	CXP_TEST_PCKTS_SENT	RC	Test packets sent on the uplink.
0x0E8	CXP_TEST_PCKTS_RECV	RO	Good test packets received on the downlink, connection 0.
0x0EC	CXP_TEST_RECV_ERRS	RO	Bad test packets received on the downlink, connection 0.

4.10 Error counters

One counter per error, each with a sticky flag in `CXP_ERRORS_HS` (high-speed downlink) or `CXP_ERRORS_LS` (uplink) that raises HS_ERR or LS_ERR. The flag says that something happened; the counter says how often. The supplied driver holds the flag positions.

Table 4-9. Error counters, one per CXP_ERRORS_HS / CXP_ERRORS_LS flag. Write 0 to clear; reading does not clear.

OFFSET	NAME	ACCESS	MEANING
0x0F0	STREAM_K_CODE_ERRS	RC	Stream packets with a bad K code.
0x0F4	STREAM_CRC_ERRS	RC	Stream packets with a CRC error.
0x0F8	STREAM_DSIZEP_ERRS	RC	Stream packets whose size does not match DsizeP.
0x0FC	STREAM_PCKT_MAX_ERRS	RC	Stream packets larger than STREAM_PCKT_MAX.
0x100	FRAME_XSIZE_ERRS	RC	Line length errors against the image header (Xsize).
0x104	FRAME_YSIZE_ERRS	RC	Frame height errors against the image header (Ysize).
0x108	PIXEL_FMT_ERRS	RC	Pixel format errors in the image header.
0x10C	CNTRL_K_CODE_ERRS	RC	Control acknowledges with a bad K code.
0x110	CNTRL_CRC_ERRS	RC	Control acknowledges with a CRC error.
0x114	CNTRL_TAG_N_EXP_ERRS	RC	Control acknowledges with a tag when none was expected.
0x118	CNTRL_TAG_EXP_ERRS	RC	Control acknowledges without the expected tag.
0x11C	CNTRL_SIZE_ERRS	RC	Control acknowledges with a size error.
0x120	CNTRL_TAG_ERRS	RC	Control acknowledges with the wrong tag.
0x124	EVENT_MSTR_ID_ERRS	RC	Event packets for another Host ID.
0x128	EVENT_MALF_ERRS	RC	Malformed event packets.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

OFFSET	NAME	ACCESS	MEANING
0x12C	EVENT_K_CODE_ERRS	RC	Event packets with a bad K code.
0x130	EVENT_CRC_ERRS	RC	Event packets with a CRC error.
0x134	HRTBT_MSTR_ID_ERRS	RC	Heartbeats for another Host ID.
0x138	HRTBT_MALF_ERRS	RC	Malformed heartbeats.
0x13C	HRTBT_K_CODE_ERRS	RC	Heartbeats with a bad K code.
0x140	LS_CMD_FIFO_EMPTY_ERRS	RC	Uplink command FIFO empty errors.
0x144	LS_CMD_SIZE_ERRS	RC	Uplink command size errors.

4.11 Statistics

Table 4-10. Statistics. RC counters take any written value: write 0 to clear.

OFFSET	NAME	ACCESS	MEANING
0x148	STREAM_PCKTS_RECV_TOT	RC	Stream packets seen.
0x14C	STREAM_PCKTS_RECV_SUCC	RC	Stream packets that ended cleanly.
0x150	STREAM_XSIZE_CNTR_ERR	RO	Words counted in the line that raised FRAME_XSIZE.
0x154	STREAM_YSIZE_CNTR_ERR	RO	Lines counted in the frame that raised FRAME_YSIZE.
0x158	VIDEO_OVF_ERRS	RC	Stream words dropped because the video path was full.
0x15C	PIX_LINE_ERRS	RC	Lines that broke the width rule of the pixel format.
0x160	FRAMES_RECV	RC	Image headers received.
0x164	HRTBT_RECV	RC	Heartbeat packets received.
0x168	LOSS_LOCK_CNT	RC	Loss of lock events, all connections.
0x16C	RATE_CHANGE_CNT	RC	Completed line rate changes.
0x170	STREAM_TAG_ERRS	RC	Stream packet tag jumps (lost packets).

4.12 Link bring-up sequence

CoaXPress discovery and configuration as the supplied driver performs it, in register terms. Camera addresses are the CoaXPress bootstrap registers.

01 **Identify the core**
Read `ID` (expect 0xA71C0A01) and `VERSION` (0x02020001 for v2.2.1). Read `HWCFG` and `VIDEO_CAP` for the transceiver, connections and the formats built.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

02 Interrupts

Clear `ISR`, enable the sources you service in `IER` (LOCKED, LOSS_LOCK, CNTRL_ACK, RATE_DONE, RATE_ERR, FRAME, the error sources), set `GLBL_IER`.

03 Discovery

Uplink at 20.83 Mb/s, untagged commands (`CXP_LS_MODE` = 0). Send ConnectionReset to the camera, then step `CXP_RATE_TRANS` through the discovery speeds until the connection locks.

04 Probe the camera

Read the bootstrap Standard register (0xC0A79AE5 for a CoaXPress camera), write a Host ID to MasterHostConnectionID and to `CXP_MASTER_ID`, read ConnectionConfigDefault for the operating speed, and negotiate the version and packet size. For CXP 2.x set `CXP_LS_MODE.TAGGED`.

05 Operating speed

Write ConnectionConfig on the camera and wait for its acknowledge, then write `CXP_RATE_TRANS` with the new speed and `APPLY`, and `CXP_LS_MODE.LS_RATE` for CXP-10 and CXP-12. Wait for RATE_DONE and LOCKED.

06 Stream setup

Write `STREAM_PCKT_MAX` with the negotiated packet size and `PIXEL_TYPE` with the camera's pixel format; check `PIXEL_TYPE.NOT_BUILT` = 0.

07 Acquire

Start acquisition through the camera's GenICam registers. FRAME fires on every image header, `FRAMES_RECV` counts frames and the image header registers show the geometry.

08 Monitor

Watch `CXP_ERRORS_HS`, `VIDEO_OVF_ERRS`, `PIX_LINE_ERRS` and `STREAM_TAG_ERRS`. A rising CRC count points at the cable, the connector or the equalizer.

The same steps with plain register accesses, for the first look at a new board:

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

```
/* base = address of cxp_host_0 in the Vivado address editor */
#define HOST(off)  (base + (off))

if (Xil_In32(HOST(0x000)) != 0xA71C0A01) return -1;   /* ID                */
u32 ver = Xil_In32(HOST(0x004));                      /* VERSION 2.2.1     */
u32 cap = Xil_In32(HOST(0x030));                      /* VIDEO_CAP         */

Xil_Out32(HOST(0x018), 0xFFFFFFFF);   /* ISR: clear everything           */
Xil_Out32(HOST(0x01C), 0x2A84);       /* IER: CNTRL_ACK, LOCKED, FRAME,  */
                                      /*      RATE_DONE, RATE_ERR        */
Xil_Out32(HOST(0x014), 1);            /* GLBL_IER                        */

/* ... discovery and camera configuration through the control channel ... */

Xil_Out32(HOST(0x028), 0x0A);         /* PIXEL_TYPE: Bayer 12-bit        */
if (Xil_In32(HOST(0x028)) & (1u << 17)) return -2;    /* not built       */
u32 frames = Xil_In32(HOST(0x160));   /* FRAMES_RECV                     */
```

The software driver supplied with the core performs these steps, including the control channel transactions and the line rate change; see Software.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 05

Example Designs and Software

The APT-C11-FMC CoaXPress card, the DisplayPort loopback and PCIe frame grabber designs, the bring-up flow and the software that comes with the core.

5.1 Evaluation hardware

The **APT-C11-FMC** is ApotheoTech's CoaXPress FMC card, built for the Host and Device cores: coax connectors, CoaXPress equalizers and uplink drivers, wired to the transceivers of the carrier board. With one card a ZCU106 runs the Host and the Device core against each other over real coax.

Table 5-1. Evaluation platforms.

BOARD	DEVICE	TRANSCEIVER	EXAMPLE DESIGNS
AMD ZCU106 + APT-C11-FMC	Zynq UltraScale+ MPSoC XCZU7EV	GTH	DisplayPort loopback, demo bitstream; PCIe frame grabber
AMD KCU116 + APT-C11-FMC	Kintex UltraScale+ XCKU5P	GTY	PCIe frame grabber
Your board	Any supported AMD device	GTH or GTY	Custom integration (NRE)

5.2 Demo bitstream

A free demo bitstream for the ZCU106 with the APT-C11-FMC runs the Host and the Device core in loopback and shows the received video on a DisplayPort monitor. It is the standard test of the cores, and the quickest way to see the link, the line rate change and the pixel formats work before you build anything.

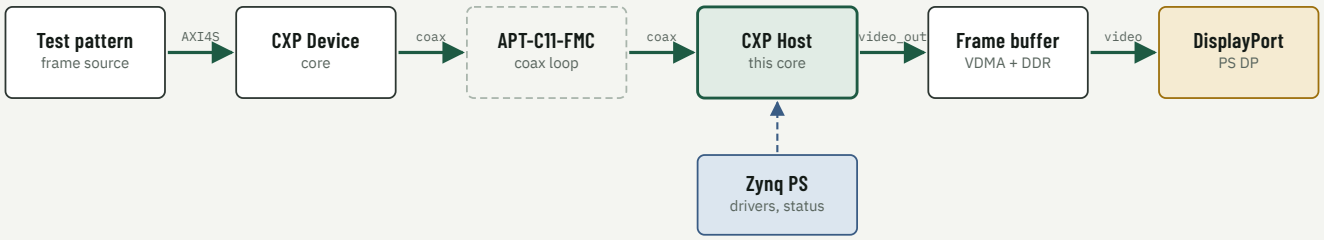
5.3 Example designs

Each example design is a complete Vivado project: the block design, constraints, a script that recreates the project, the transceiver wrapper and the software.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

DisplayPort loopback

Included with Host + Device

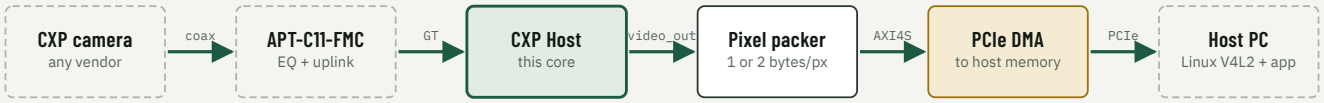


A test pattern feeds the CoaXPress Device core, the link runs over coax through the APT-C11-FMC, and the Host core's video goes through a frame buffer to the DisplayPort output of the Zynq MPSoC. The processor runs discovery, changes speed and switches pixel formats. Free to anyone who licenses both cores.

Cores Host and Device **Platform** ZCU106 + APT-C11-FMC **Software** bare-metal, DisplayPort

PCIe frame grabber

Add-on



A CoaXPress frame grabber on a PCIe card. The Host core's video is packed to 1 or 2 bytes per pixel, following `pixel_type_out`, and written into host memory by a PCIe DMA engine. All core control runs from the PC over PCIe. Includes a Linux V4L2 driver and a capture application.

Platforms KCU116, ZCU106 **Host** Linux, V4L2 **Link** PCIe

Custom integration

NRE

Work directly with ApotheoTech on your frame grabber: your board and FMC, 2 and 4 connection cameras, a pipeline behind the core (debayer, ISP, encoder), or a CoaXPress bridge to PCIe, Ethernet or SDI.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

5.4 Bring-up flow

01 Recreate the project
Run the example design's Tcl script in Vivado. It adds the IP repository, builds the block design and applies the constraints.

02 Choose the build
In the IP GUI pick the transceiver, set the AXI4-Lite clock, switch on the pixel layouts and bit depths your cameras use, and set pixels per beat and bits per component to match the logic behind `video_out`.

03 Build and export
Generate the bitstream and export the hardware platform for Vitis.

04 Build the application
Create the Vitis platform and application, add the example sources and the driver.

05 Run
Program the board and plug in the camera. The console prints the core version and build, runs discovery and moves to the camera's operating speed.

06 Check the link
The connection locks, frames are counted and the error counters stay at 0. CRC errors point at the cable, connector or equalizer; a line width error at a pixel format that does not match the camera.

5.5 Software

The core comes with a software driver for setup and control, supplied on purchase, for MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC processors. It identifies the core and its build, services the interrupts, runs control channel reads and writes on the camera, performs discovery and the line rate change, selects the pixel format and reads the counters. The example designs use it, so they double as working references for your own application. The PCIe frame grabber add-on adds a Linux V4L2 driver and a capture application that control the core over PCIe.

5.6 Verification

The Host core is verified against the ApotheoTech Device core over a model of the link, and on its own in a UVM 1.2 testbench, with a link monitor that checks IDLE spacing and packet tags on every word.

- Both cores back to back: identification, control reads and writes (untagged at discovery, tagged at the operating speed), interrupts, every pixel format of the build, events, heartbeat, triggers in both directions, connection test, line rate change errors with recovery, CRC error injection and a stalled video sink.
- The pixel path is checked for 11 bus builds and every format each carries, up to 25: the link words against a bit-serial model of CoaXPress 2.1, and the beats out of the Host against the UG934 beat, with gaps and stalls on every FIFO and the throughput table enforced.
- The line rate change is checked against a transceiver model for every failure: DRP not answering, reset not connected, PLL never locking, a request during a change, and a reset during a change.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

- `pixel_type_out` is checked at every start of frame against the format of that frame, with the ApotheoTech pixel packer behind the core.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

SECTION 06

Resources and Ordering

Device support, what each pixel format costs, the licensing configurations, what you receive and how to evaluate and order.

6.1 Supported devices

Table 6-1. AMD device and transceiver support.

FAMILY	TRANSCEIVER	SPEEDS	STATUS
Zynq UltraScale+ MPSoC, including Kria K26	GTH (GTHE4)	CXP-1 to CXP-12	Example designs
Kintex UltraScale+	GTY (GTYE4), GTH (GTHE4)	CXP-1 to CXP-12	Example designs
Other UltraScale+ devices	GTH, GTY	CXP-1 to CXP-12	Contact ApotheoTech
7 series and other families	Per family		NRE engagement

6.2 Resource utilization

The pixel formats you switch on set most of the size difference between builds. The table below is an estimate of the pixel path block alone, so you can see what a format costs; read it as one build against another. A Vivado utilization report for your build, including the receive path, the protocol handling and the FIFOs, comes with the evaluation.

Table 6-2. What a format switch costs: estimate of the pixel path block alone at 4 pixels of 16 bits per beat, UltraScale+. Read it as the size of one build against another; it is not a Vivado utilization report.

FORMATS BUILT	HOST LUT	HOST FF	DEVICE LUT	DEVICE FF	DEVICE BRAM
Mono / Bayer, 8-bit only	127	86	98	91	
Mono / Bayer, 8, 10 and 12-bit	406	275	413	289	
Mono / Bayer, every depth (default)	841	510	792	489	
adds YCbCr 4:2:2	1,051	707	883	625	
adds YCbCr 4:2:2 and 4:2:0	1,089	708	933	701	2
adds RGB	1,194	836	921	690	
adds RGB and YCbCr 4:4:4	1,263	836	1,160	690	
everything (25 formats)	1,389	1,034	1,207	902	2

- Bit depths are the larger lever: each depth in **Bit depths on the link** is a gearbox of its own. A product that only runs 8 to 12-bit saves about half of the pixel path.
- RGB and YCbCr 4:4:4 share one layout block, YCbCr 4:2:2 and 4:2:0 the other; switching off one of a pair saves little.
- The video FIFO is `tdata` + 2 bits wide: one BRAM36 at 512 beats of the default 64-bit bus, three for the 192-bit bus.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

6.3 Licensing configurations

Table 6-3. The CoaXPress cores are licensed in four configurations.

CONFIGURATION	CONTENTS	FOR
Host Only	CoaXPress 2.1 Host core	Frame grabbers and embedded vision systems that take any CoaXPress camera
Host + Test Device	Host core and a Device core restricted to its internal test pattern, without a video input	Capture card developers who need a link partner for test and production
Device Only	CoaXPress 2.1 Device core	Camera makers
Host + Device	Both cores; includes the DisplayPort loopback example design	Complete camera-to-grabber systems and bridges

6.4 Deliverables

Table 6-4. What a license includes.

IP core	Encrypted netlist for the target FPGA family and transceiver, packaged for Vivado IP Integrator with its customization GUI
Transceiver wrapper	GTH or GTY transceiver wrapper set up for CoaXPress, with the line rate tables the core uses
Integration guide	Interface descriptions, register map, integration checklist
Instantiation templates	Verilog and VHDL wrapper templates
Example designs	Complete Vivado projects for the licensed configuration
Software	Driver for setup and control on MicroBlaze, Zynq-7000 and Zynq UltraScale+ MPSoC, plus the example applications
Updates and support	One year of updates and email support included; renewal afterwards

6.5 Evaluation and ordering

Evaluate

The free ZCU106 demo bitstream runs Host and Device in loopback with the APT-C11-FMC. Ask for an evaluation of your build.

License

Perpetual license with one year of updates. Add-on example designs and NRE engineering on request.

Engineering services

Integration on your board, 2 and 4 connection builds, ISP and encoder pipelines, complete frame grabbers and cameras.

© 2026 ApotheoTech LLC | apotheotech.com | info@apotheotech.com

CONTACT

ApotheoTech LLC

Email: info@apotheotech.com

Web: apotheotech.com

For pricing, evaluation access or technical questions, email us with your camera, speed, pixel formats and target device.

Related ApotheoTech products: the CoaXPress 2.1 Device IP core, the SLVS-EC Receiver IP core, the APT-C11-FMC CoaXPress card and the Aper-Oculus Kria K26 carrier board.

6.6 Revision history

Table 6-5. Datasheet revisions.

REVISION	DATE	CHANGES
1.0	November 2026	First release, for IP v2.2.1.

6.7 Notices

CoaXPress is a trademark of the Japan Industrial Imaging Association (JIIA). JIIA CXP-001-2021 is published by the JIIA. GenICam is a trademark of the European Machine Vision Association (EMVA). AMD, Xilinx, Zynq, Kria, Kintex, UltraScale, Vivado and Vitis are trademarks of Advanced Micro Devices, Inc. All other names are the property of their respective owners. Specifications are subject to change without notice. This document describes the IP core and does not grant any license.